Stacked Ge$_2$Sb$_2$Te$_5$/GeTe Multi-level Phase-change Memory with Asymmetric Double-Heater

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Abstract—An asymmetric double-heater structure is proposed into the traditional stacked layer phase-change memory (PCM) for the first time. It contains no barrier layer. The superior multi-level storage (MLS) is verified in this structure by numerical simulation. Temperature at the interface of two phase-change materials is greatly reduced by reasonably choosing the heater radius, which is beneficial for less atomic interdiffusion at the interface, thus more stable MLS. Device performance can be optimized through material thickness trade-off. Hence, this structure is a candidate utility for the future MLS device.

Keywords—asymmetric double-heater; MLS; interdiffusion; temperature distribution

I. INTRODUCTION

Due to its non-volatile, low power consumption, phase-change memory (PCM) has become the most promising next generation memory. Pursuing the higher storage density is one of the most important requirement in PCM development, then multi-level storage (MLS), which can raise the storage density by increasing the logical number of storage unit, is presented to solve this challenge [1].

The stacked layer structure is usually utilized in multi-level PCM owing to the large difference of resistance switch range of two materials. The phases of two materials switch orderly on account of the different thermal conductivity, electric conductivity and melting temperature ($T_m$), generating low, median and high resistance (LR, MR, HR) state respectively.

Seen from the reliability, a stable MR is needed for MLS, which is mainly affected by the atomic interdiffusion around the two different materials interface [2]. An added barrier layer is usually used to solve it [3, 4]. In the previous structure, phase change region almost involves the whole layer and energy consumption becomes larger compared to mushroom active region structure. Meantime, the barrier layer adds more uncertain interface contact problems [5, 6]. In our work, a stacked Ge$_2$Sb$_2$Te$_5$/GeTe structure with asymmetric double-heater is proposed, to remove the barrier layer and greatly reduce the interdiffusion between the two materials.

II. DEVICE STRUCTURE

The proposed multi-level PCM 2D structure is shown in Fig.1. The phase change materials are Ge$_2$Sb$_2$Te$_5$ (GST) and GeTe (GT), TEC and BEC are W, heaters are TiN. The electro-thermal model is presented by solving Laplace equation (1) and the Joule heating transfer equation (2):

$$\nabla \cdot \sigma (r, z, t) \nabla \phi = 0. \tag{1}
$$

$$\nabla \cdot (K(r, z, t) \nabla T) + Q = \rho C \frac{dT}{dt}, \tag{2}
$$

where $\sigma$ is electrical conductivity, $K$ is thermal conductivity, $C$ is heat capacity, and $\rho$ is material density. The phase-change material parameters are shown in TABLE I and calibrated with [7]. Finite element modeling by COMSOL is applied to simulate the device thermoelastic characteristic and phase change process in RESET operation.

III. RESULTS AND DISCUSSION

Fig.2 shows the temperature distribution after a current pulse. The highest temperature is located at the interface between the phase-change material and the heater, where phase-change happens. Phase distribution under increasing current density (J) is shown in Fig.3. GST switches to the amorphous state first because of its low $K$, $T_m$ of GST and GT are 889K and 998K, respectively and high $\sigma$. After the GST heater is covered by the GST amorphous area, device resistance rises to MR. When it increases up to the HR threshold current, the GT end begins the same process, then the cell switches to HR state.

Fig.4 presents the temperature distribution along the y-axis shown in Fig.2. As current increases, the lowest temperature point is always located at the interface. Compared to no heater groups, the asymmetric double-heater structure can decrease interface temperature effectively. Even as $J=8.5e^4 A/m^2$, the cell is on HR state and the interface temperature is still lower than 650K. According to [2], the interdiffusion is mild under the relative low temperature. Hence, it is verified that this structure has the superior ability to suppress the interdiffusion at the interface and keep good reliability.

R-I curves with different GT heater radius ($R_{GT}$) are shown in Fig.5. GST heater radius ($R_{GST}$) is set to 40nm. The less $R_{GT}$ leads to more concentrated current and GT will change more quickly, even simultaneously with GST. As for $R_{GT}=8$nm, there is only one resistance switch and no MR, so it is hard to achieve MLS when the $R_{GT}$ is not large enough. Large threshold current window is preferred for current programming, which can be achieved by increasing $R_{GT}$. The
GST amorphous region will expand to the interface as the current increases, leading to the increasing whole resistance. If GT changes too slowly, the resistance of GST amorphous area is close to GT amorphous resistance. As for $R_{GT}=12\text{nm}$, the whole resistance rises slowly from MR to HR. There is no second resistance switch. It is also hard for MLS to take place. Under this condition, interdiffusion is severe and power consumption is large. Therefore, we should give $R_{GST}$ a trade-off. As is shown in Fig.6, the interface temperature as well as the rising ratio goes down as the material thickness gets thicker, which is preferable for the device stability. But thicker material leads to higher resistance. So we can optimize the structure performance by trading off material’s thickness and low device resistance.

IV. CONCLUSION

In this work, an asymmetric double-heater stacked PCM structure is proposed. The temperature at the two different materials interface is greatly suppressed in this structure, which leads to suppressed atomic interdiffusion and stable MLS. The geometry optimization is discussed, and results show that it is important to optimize of heater radius and material thickness for performance improvement.

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