A Highly Stable Biside Gate Driver Integrated by IZO TFTs
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Abstract—This brief presents a new gate driver integrated by In–Zn–O thin-film transistors (IZO TFTs), including a clock-controlled inverter and an additional stabilized module. The biside driving method is used in the proposed gate driver, which will be allocated on both sides of the panel to drive the odd and even lines of pixel array, respectively. Thus, the space symmetry of the panel can be fully utilized for high resolution displays. The output signal of the biside gate driver can be generated stably up to 480th stage with a good noise-suppressed characteristic. The measured power consumption for one stage of the proposed gate driver is 0.5 mW with the clock frequency as 50 kHz. It is shown that the proposed gate driver can output a 3-μs pulsewidth with a good stability under 120-h test. Furthermore, a 3-in demonstration panel of 320*480 AMOLED display by the IZO TFTs process is fabricated to verify the function of the proposed biside gate driver.

Index Terms—Bi-side, gate driver, In–Zn–O thin-film transistors (IZO TFTs).

I. INTRODUCTION

HERE are several benefits for the gate driver integrated by thin-film transistors (TFTs) in flat panel display, such as simpler process, lower cost, thinner thickness, and narrower bezel [1]–[3]. In recent years, metal–oxide TFTs (MO TFTs) of which the active layer may be zinc-oxide (ZnO) [4], [5], indium–gallium–zinc-oxide [6], [7] or indium–zinc-oxide (IZO), which our group focuses on [8]–[10], have gained much attention due to their high mobility, low sub-threshold voltage swing, high current ON/OFF ratio, and good process compatibility with a-Si TFTs. However, unlike a-Si: H TFTs or p-Si TFTs, MO TFT operates in a depletion mode and its threshold voltage is about zero [4]–[10]. As a result, there are some difficulties for MO TFTs to integrate the gate driver compared with a-Si: H TFTs or p-Si TFTs.

Several gate driver circuits integrated by MO TFTs have been developed [11]–[14]. Long-term operation stability for the gate driver with a large number of stages in series connection is considerably important for its application in the flat panel display. However, this issue has been taken into account by few circuits. In addition, narrower bezel of panel is needed for users’ visual experience, especially in the mobile application. Thus, the area on the glass left for the scan driver is limited. The space symmetry of panel can be fully utilized if the gate driver is allocated on both sides of panel to drive the odd and even lines of pixel array, respectively. Hence, the gate driver realized by this method is named as biside gate driver.

In this brief, a new biside gate driver integrated by IZO TFTs is proposed. It is shown that the proposed gate driver can work stably through a 120-h test. Moreover, a demonstration AMOLED panel with 480 stages is also fabricated to verify the effectiveness of the proposed gate driver.

II. FABRICATION AND CHARACTERISTICS OF IZO TFTs

The IZO TFTs integrated for the proposed gate driver were fabricated as follows [10]. A 200-nm molybdenum (Mo) gate metal film was deposited onto glass substrate. Then, a 200-nm-thick SiO2 gate insulator film was deposited by plasma-enhanced chemical vapor deposition at 310 °C as insulator. The IZO active layer with the In:Zn ratio as 1:1 was deposited on the insulator SiO2 by radio frequency magnetron sputtering with thickness of 30 nm. Then, an etch stop layer used for protecting the active layer was fabricated by dry-etch. The source/drain electrodes were deposited by dc sputtering and patterned by wet-etch. Finally, SiO2 passivation layer was formed to protect the TFT device.

Fig. 1 shows the transfer characteristics of the IZO TFTs (W/L = 20 μm/10 μm) extracted per hour under negative-bias temperature stress (NBTS) and positive-bias temperature stress (PBTS) for 12 h. The conditions of PBTS are $V_g = 15$ V, $V_d = 10$ V, and that of NBTS are $V_g = -15$ V, $V_d = 10$ V. It is shown that the field-effect mobility, threshold voltage, and subthreshold swing at the initial condition are $13.7 \text{cm}^2/(\text{V} \cdot \text{s})$, 0.1 V, and 240 mV/decade, respectively. In addition, the ON/OFF current ratio is over $10^9$ revealing a good property. For 12-h stress, the whole threshold voltage shift under NBTS with a value of $-1$ V is more serious than...
Fig. 1. Measured transfer characteristic of IZO TFTs (W/L = 20 μm/10 μm) under (a) NBTS and (b) PBTS.

Fig. 2. Proposed gate driver. (a) Schematic view of a single stage. (b) Timing diagram. (c) Block diagram.

that under PBTS with a value of 0.5 V. It should be indicated that the IZO TFTs work in the depletion mode rather than in the enhancement mode.

III. PROPOSED GATE DRIVER CIRCUIT OPERATION

Fig. 2(a)–(c) shows the schematic view of the proposed gate driver with a single stage, its timing diagram, and the block diagram, respectively. It is shown that the proposed gate driver circuit is driven by three clock signals (i.e., CLK1, CLK2, and CLK3) and employs three power supplies (VDD, VSS, and VSSL). T1a and T1 form an STT structure and are used to input previous stage shift register signal [13]. T5 and T7 are the pull-up TFTs, whereas T6 and T8 are the pull-down TFTs.

T9 is a feedback TFT, which transfers the carry output signal COUT(N) to the node A between input TFTs T1a and T1. T3, T4, and T4a form the inverter to generate Qb, i.e., the inverting signal of Q. Note that this inverter may be called as clock-controlled inverter since T3 is controlled by CLK1. Furthermore, T2 and T2a form a stabilized module, which is used to stably maintain Qb as low level when the output signal OUT(N) is high. The capacitors C1 and C2 are used to stabilize the signals of OUT(N) and COUT(N). The operation of the proposed gate driver circuit is divided into three periods as follows.

A. Start Signal Input Period

The clock signals CLK1 and CLK3 remain low, whereas CLK2 switches to high. So, the start signal VIN(N) is input to node Q through the input TFTs T1 and T1a, which turns on the pull-up TFTs T5 and T7. T3 is kept OFF by the low level of CLK1. Meanwhile, node Qb discharges to VSSL since T4 and T4a are turned on by the high level of VIN(N). Thus, the pull-down TFTs T6 and T8 are turned OFF. The output signal COUT(N) and OUT(N) keep low in this period due to the low level of CLK3. Note that the direct current path can be avoided in our proposed clock-controlled inverter compared with the conventional diode-connected inverter when the output of the inverter is low [14]–[16].

B. Holding Period

CLK1 and CLK3 remain low, whereas CLK2 and VIN(N) switch to low to turn off T1a, T1, T4a, and T4. However, node Q keeps high due to C1 and node Qb keeps low due to C2. It should be pointed out that the other side of the gate driver just generates output signals during this period. As a result, the biside driving method can be realized by the addition of such holding period.

C. Output Generation Period

CLK1 and CLK2 keep low, whereas the clock signal CLK3 switches to high. Then, the input TFTs T1 and T1a are kept off. The pull-up TFTs T5 and T7 are kept on due to the high level of node Q. COUT(N) and OUT(N) output high because of the high level of CLK3. Furthermore, the voltage of node Q is bootstrapped up to a higher level due to the coupling effect of C1. It should be indicated that the output signal OUT(N) is generated to drive the Nth row line, whereas the signal COUT(N) is provided as the start signal [VIN(N)] of the next stage. The feedback TFT T9 is turned on by COUT(N) signal and the high level of CLK3 is exported to the node A to prevent the leakage current of T1. Meanwhile, COUT(N) signal is also exported to turn on T2 and T2a, so that node Qb is kept as VSSL to maintain T6 and T8 off. This feedback method can effectively suppress the bootstrap effect of the parasitic capacitor Cgs of T6 and T8.

D. Reset Period

Primarily, CLK3 switches to low, so the voltage of node Q is bootstrapped down to the lower level as same as that in
the holding period. Meanwhile, the output signals OUT(N) and COUT(N) turn low due to low level of the CLK3. Next, Qb is charged to VDD through T3 as CLK1 switches to high. Then, T1a and T1 are turned on when CLK2 becomes high. Consequently, node Q is discharged to VSSL through T1a and T1 because of the low level of VIN(N).

IV. RESULTS AND DISCUSSION

Fig. 3 shows the optical image of the proposed gate driver circuit. The area of a single stage is 1495 μm × 258 μm. In addition, the design specifications are described in Table I. Note that the size of T7 and T8 should be large enough to guarantee the driving ability. The equivalent load of the row line in the panel (320 × 480) is R = 3 kΩ and C = 90 pF. The pulselwidth of start signal is 20 μs. Fig. 4 shows the output waveforms of the proposed biside gate driver with 480 stages. The first stage is denoted by the green line, whereas the 480th stage is denoted by the yellow line. It is shown that the high level of the output signal is close to VDD and its low level keeps at VSS with little ripple during the frame time. Furthermore, it is observed that the 480th stage can generate the output signal with little distortion compared with the first stage. Therefore, the expected shift function with a good noise-suppressed characteristic can be well realized by our proposed biside gate driver.

Long-term operation is a key factor for gate driver applied in the flat panel display. Fig. 5 shows the characteristics of long-term operation for the proposed gate driver in the test unit with the load R = 100 Ω and C = 30 pF. It should be noted that the pulselwidth of the output waveform in this experiment is about 3 μs, which can easily meet the requirement of ultrahigh definition display [UHD, 3840(RGB)*2160] at a frame rate 120 Hz. The blue-solid line denotes the output waveform of the initial time, whereas the red-dashed line denotes the waveform after 120-h operation. It can be seen that the output waveform after 120-h operation is nearly same as that of the initial condition. In a word, the proposed gate driver can achieve a good stability for long-term operation.

The power consumption of the gate driver contains two parts: 1) the dynamic consumption and 2) the static consumption, and it can be expressed as [17]–[19]

$$P_G = K * C_{CLK} * (V_H - V_L)^2 * f_{CLK} + V * I.$$  (1)

The first term is the dynamic one, where K is a fixed coefficient, C_{CLK} is the parasitic capacitance of the gate driver circuit, f_{CLK} is the operating frequency of clock signal, V_H and V_L are high level and low level of clock signals, respectively. The second term is the static one. Note that the dynamic one occupies the most of the whole power consumption compared with the static one. It is obvious that the power

### TABLE I

**Design Parameters of the Proposed Gate Driver**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage level of clock signals</td>
<td>8–12</td>
</tr>
<tr>
<td>CLK1, CLK2, CLK3(V)</td>
<td></td>
</tr>
<tr>
<td>Voltage level of power line VDD, VSS, VSS (V)</td>
<td>12, -8, -6</td>
</tr>
<tr>
<td>Circuit area</td>
<td>1495μm*258μm</td>
</tr>
<tr>
<td>(W/L)T1, T1a (μm/μm)</td>
<td>240/10</td>
</tr>
<tr>
<td>(W/L)T2, T2a (μm/μm)</td>
<td>20/10</td>
</tr>
<tr>
<td>(W/L)T3, T4, T4a (μm/μm)</td>
<td>100/10</td>
</tr>
<tr>
<td>(W/L)T5 (μm/μm)</td>
<td>240/10</td>
</tr>
<tr>
<td>(W/L)T6 (μm/μm)</td>
<td>80/10</td>
</tr>
<tr>
<td>(W/L)T7 (μm/μm)</td>
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<tr>
<td>(W/L)T8 (μm/μm)</td>
<td>500/10</td>
</tr>
<tr>
<td>(W/L)T9 (μm/μm)</td>
<td>10/10</td>
</tr>
<tr>
<td>C1 (pF)</td>
<td>2</td>
</tr>
<tr>
<td>C2 (pF)</td>
<td></td>
</tr>
<tr>
<td>Test temperature(°C)</td>
<td>25</td>
</tr>
</tbody>
</table>
can output a 3
is 0.5 mW with f
power consumption for one stage of the proposed gate driver
consumption can be considerably reduced by reducing the
parasitic capacitance and operating frequency. The measured
power consumption for one stage of the proposed gate driver
is 0.5 mW with \( f_{\text{CLK}} \) as 50 kHz.
As shown in Fig. 6, a demonstration panel of 320 \( \times \) 480 AMOLED display by IZO TFTs process is fabricated to verify
the function of the proposed biside gate driver. In addition,
its specifications are listed in Table II. It is shown that the
proposed biside gate driver can work stably up to 480 stages
with fine display quality.

V. CONCLUSION
In this brief, a new biside gate driver integrated by IZO TFTs is presented, which includes a clock-controlled inverter and an additional stabilized module. It is observed that the output signal of the gate driver can be generated stably up to 480th stage with little distortion. The measured power consumption for one stage of the proposed gate driver is 0.5 mW with \( f_{\text{CLK}} \) as 50 kHz. The proposed gate driver can output a 3 \( \mu \)s pulselwidth, which can easily meet the requirement of UHD [3840(RGB)*2160] display at a frame rate 120 Hz. Moreover, it is shown that the proposed gate driver can achieve a good stability under 120-h test. At last, the function of the proposed biside gate driver is also verified by a 192 PPI demonstration panel of 320 \( \times \) 480 AMOLED display with fine display quality.

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Authors’ photographs and biographies not available at the time of publication.