Multicast-Based Testing and Thermal-Aware Test Scheduling for 3D ICs with a Stacked Network-on-Chip

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Abstract—A 3D stacked network-on-chip (NOC) promises the integration of a large number of cores in a many-core system-on-chip (SOC). The NOC can be used to test the embedded cores in such SOCs, whereby the added cost of dedicated test-access hardware can be avoided. However, a potential problem associated with 3D NOC-based test access is the emergence of hotspots due to stacking and the high toggle rates associated with structural test patterns used for manufacturing test. High temperatures and hotspots can lead to the failure of good parts, resulting in yield loss. We describe a unicast-based multicast approach and a thermal-driven test scheduling method to avoid hotspots, whereby the full NOC bandwidth is used to deliver test packets. Test delivery is carried out using a new unicast-based multicast scheme. Experimental results highlight the effectiveness of the proposed method in reducing test time under thermal constraints.

Index Terms—On-chip networks, NOC core testing, 3-D stacked NOCs, thermal-aware test delivery, unicast-based multicast.

1 INTRODUCTION

A network-on-chip (NOC) has emerged as a promising communication paradigm for core-based system chips [5], [23]. A 3-dimensional (3D) network-on-chip, the combination of NOC and die-stacking 3-D IC technology [9], [28], is motivated by the need to achieve low latency, low-power consumption, and high network bandwidth. Testing complex and embedded NOCs is therefore a challenging problem.

An inefficient solution to the NOC testing problem does not use the full NOC bandwidth for testing and instead delivers tests to cores sequentially, which is likely to increase test time considerably and thereby increase test cost [7]. Reuse of the communication platform [8] is a cost-effective technique for targeting the cores in a multicore chip with a NOC. Test solutions have targeted routers, cores [7], [8], and interconnects [14]. A number of design for testability (DFT) techniques have been proposed for NOC testing [4], [9], [25], [33].

We introduce some related concepts first. A unicast scheme delivers a packet from a single core, called the source, to a single destination. A multicast scheme delivers a packet from a single core called the source to multiple cores in the NOC [22], [3]. A unicast-based multicast scheme completes multicast by using multiple unicast steps, therefore, it is not necessary to modify the unicast router architecture [22].

Let the address of a node \( x \) be represented by \( (\sigma_1(x), \sigma_2(x), \ldots, \sigma_n(x)) \). The binary relation dimension-order, denoted \( <_d \), is defined between two nodes \( x \) and \( y \) as follows: \( x <_d y \) if and only if there exists an integer \( j \) such that \( \sigma_j(x) < \sigma_j(y) \) and \( \sigma_i(x) = \sigma_i(y) \) for all \( i \), \( 0 \leq i \leq j - 1 \). For any set of node addresses, they can be arranged in a unique sequence according to the \( <_d \) relation. A sequence of nodes \( x_1, x_2, \ldots, x_m \) is a dimension-ordered chain if and only if, (1) \( x_i <_d x_{i+1} \) for \( 1 \leq i < m \), or (2) \( x_i <_d x_{i-1} \) for \( 1 < i \leq m \).

Let \( u, v, w \) and \( z \) meet \( u <_d v <_d w <_d z \), two unicast packets can be delivered from \( u \) to \( v \), and from \( w \) to \( z \) concurrently without any joint link [22]. Two unicast packets can also be delivered from \( v \) to \( u \), and from \( z \) to \( w \) with disjoint link by using \( X-Y \) routing in a 2D mesh/torus. The \( X-Y \) routing in a 2D torus requires two virtual channels unlike deterministic routing in a 2D mesh, which uses just a single virtual channel.

Fig. 1(a) presents an example 6×6 mesh. Let the automatic test equipment (ATE) be connected to the core of node (3,0) in the 2D stacked design. A test packet must be delivered to the eight nodes as shown in Fig. 1. The dimension-ordered chain of the destination is: \((0,0), (1,1), (1,2), (1,4), (2,0), (3,1), (5,3), (5,8)\). Fig. 1(b) presents the 3-D stacked NOC. The test packet delivery process requires four unicast steps to deliver the test packet to all destinations.

The dimension-ordered chain with eight destinations is contained in the header flits and forwarded to node \( v_5 \) from the core connected to the ATE in the first unicast step. The test packet with the four ordered destinations \((v_1, v_2, v_3, \text{ and } v_4)\) is forwarded to \( v_4 \) in the second...
unicast step, while the test packet with \( v_7 \) and \( v_8 \) is forwarded from \( v_5 \) to \( v_7 \) in the third step, and the test packet from \( v_5 \) with \( v_6 \) is sent to \( v_6 \) in the fourth step. Similarly, the test packet at \( v_5 \) is recursively forwarded to all destinations \( v_1, v_2, \) and \( v_3 \). It is found that no channel competition occurs in steps 3 and 4 as shown in Fig. 1(a).

Previous methods [7], [8], [9] sent separate test data packets to different cores, which can lead to high test time. Test data volume can also be excessive. Consider a NOC with with one hundred cores. There may exist a very small number of different classes of cores in the NOC [39]. Xiang et al. in [34] proposed a unicast-based multicast scheme for test delivery to logic cores using the NOC as the interconnect fabric. All identical cores share the same test packets. A test packet can be multicast to all identical cores. Test responses are collected along the reverse paths of the multicast tree. A drawback of [34] is that thermal constraints [13] are not considered. It is essential to consider the thermal issue in 3-D stacked NOCs carefully, which can introduce hotspots and cause the performance and reliability problems [1], [6], [20], [28], [29], [32], [36], [37]. Moreover, the scenario of a 3D stacked chip (with a 3D NOC) was not considered and output responses must be sent back to the ATE immediately after the test vector has been applied. Finally, the method in [34] did not describe any DFT architecture for global test control.

While the paper is targeted for test delivery reduction for NOC testing, thermal-aware test scheduling, low-power scan at core level, and test response compaction, the focus here is to reduce the peak temperature. Peak temperature of cores is closely related to power consumption. Scan testing inside cores contributes the most to power consumption of a NOC, therefore, a new low-power testing scheme is proposed. Power consumption in the NOC includes test packet delivery and response packet delivery. Therefore, delivery of test response packets contributes around half of test power consumption in the NOC, which is the reason why we propose a unicast-based multicast scheme. The focus of the work is to reduce peak temperature and test data volume of the ATE.

A test set can be generated for different classes of cores separately. Each test packet can be delivered to all cores in the corresponding class by using the proposed unicast-based multicast scheme. Many cores differ only slightly in terms of the logic implementation; we refer to these as similar cores, where these cores can still share the most test packets. Two similar cores can be merged into the same circuit. Tests of two cores can be generated on the merged circuit like the method presented in [34]. The new method also works when the NOC contains completely different cores. In this case, the unicast-based multicast scheme degrades to a unicast scheme.

Power consumption inside cores during test application is a major contributor to test power consumption in a NOC-based system. It is therefore necessary to combine an efficient low-power scan testing scheme with the NOC core testing method. A new low-power scan testing scheme is presented in this paper to reduce power consumption for each core. The test responses are compacted by the on-chip X-tolerant multiple-input signature-register (MISR) unlike previous methods [7], [8], [34]. The compacted test responses in the MISR are delivered back to the ATE after all test vectors have been applied.

A new thermal-aware test scheduling scheme is also proposed by using a unicast-based multicast problem. Test packet delivery is optimized to avoid hotspots in the NOC, which can mitigate the thermal problem to a large extent. We assume that the network architecture for the 3-D NOC is a 3-D mesh, which is reasonable for the current technology [17], [21], and the 3-D NOC is designed based on the channel overlap routing algorithm. Therefore, test packet delivery conforms to the channel overlap scheme. The proposed method can be applied to NOCs designed by any other routing algorithms. For 3-D interconnects with limited vertical TSVs, the routing schemes, such as, the one in [18], can be used to deliver test packets.

The following materials are completely new compared to the conference version [37]: (1) the DFT control logic as shown in Fig. 5 to implement the proposed NOC core testing scheme is completely new. The scan architecture in [37] cannot provide pattern-independent low-power testing. That is, the DFT architecture and scan chains
are constructed based on a test set. However, the new method does not require any test set. (2) The test response collection scheme in Section 5 is also new.

In the rest of this paper, we first present preliminaries in Section 2. The NOC core testing problem is formulated as a new unicast-based multicast problem in Section 3. A new low-power scan testing scheme and the new DFT architecture are proposed to control NOC testing based on a new MISR-based response compaction technique in Section 4. Section 5 shows how the test responses are compacted and delivered back to the ATE along the reverse paths of the unicast-based multicast scheme. Experimental results in Section 6 show that the proposed method can effectively reduce test cost and test data volume, which can also greatly reduce the peak temperature. The paper is concluded in Section 7.

2 Related Work

Reuse of the communication platform [7], [8] is a cost-effective technique based on the use of existing interconnects and routers in the NOC. Cota et al. [7] proposed a technique for reuse of the communication platform for test data and test response delivery. An algorithm based on the list-scheduling technique was proposed to minimize the test cost. The method in [14] exploits the inherent parallelism of the data transport mechanism to reduce the test cost for interconnect testing and the test application time. Test scheduling algorithms were developed based on a unicast scheme and a multicast scheme for sequential and concurrent test data transport. Techniques were proposed to improve interconnect reuse for NOC testing [8], [9], [33]. Cota and Liu [8] proposed a new test scheduling scheme for NOC testing with multiple-port automatic test equipment (ATE).

Thermal-aware test scheduling techniques have been proposed [1], [6], [20], [28], [29], [37] for test scheduling of SOCs. The method in [28] introduced a technique for rapid generation of safer test schedules without time-consuming thermal simulations. Liu et al. [20] proposed a thermal-aware test scheduling scheme for NOCs by using variable clock frequencies; this approach suffers from implementation challenges and may not be cost-effective. Samaly and Harmanani [29] proposed an optimal integer linear programming formulation and a simulated annealing (SA) solution to thermal and power-aware test scheduling of cores in a NOC-based SOC using multiple clock rates. Thermal-aware schemes have been proposed for scan-based BIST and scan testing in [32], [36] to reduce peak temperature.

Forese et al. [12] proposed a new test compression scheme for core testing, where only the seeds are delivered to the cores. A test-delivery optimization algorithm was proposed by Agrawal et al. in [2] for NOC-based SOCs with hundreds of cores by using a new dynamic programming model. Ramdas and Sinanoglu in [27] proposed a comparison-based test access mechanism (TAM) that is capable of handling spare identical cores. Yuan, et al. in [40] evaluated the cost of using NoC as TAM and compared to the one with dedicated bus-based TAM in terms of testing time, DFT area cost, test reliability and test control complexity. Li, et al in [19] managed to achieve a shorter test time under power constraints through wrapper design and interleaved test scheduling without manipulating test frequencies. A comprehensive end-to-end solution was proposed for error correction, data collection, and defect diagnosis and replacement for on-chip networks in Shamshiri and Cheng [30]. They proposed a new model to evaluate the yield and cost of a NOC-based multicore chip [31].

We assume that the NOC is designed by the channel overlap routing scheme [35]. The channel overlap scheme is the baseline routing scheme for the proposed multicast scheme. The proposed unicast-based multicast scheme can also be applied to NOCs implemented by other routing schemes, such as dimension-order routing, turn model, or odd-even turn model.

3 Thermal-Aware Test Scheduling

We use a new unicast-based multicast scheme to deliver test packets as presented in Fig. 2. Unlike the previous unicast-based scheme [22], the multicast source is involved in the test delivery process only in the first unicast step. Our method puts all destinations in the header flits, where all destinations are distributed to the intermediate destinations in the process of multicast. A thermal-aware test scheduling scheme is proposed in Subsection 3.2, and a new unicast-based broadcast test delivery scheme is presented for a NOC with a single class of cores in Subsection 3.3.

3.1 Unicast-Based Multicast for 3-D NOCs

Let \( u, v, w \) and \( z \) meet the dimension-order chain relation \( <_d \), that is, \( u <_d v <_d w <_d z \), two unicast packets can be delivered from \( u \) to \( v \), and from \( w \) to \( z \) concurrently without any joint link [22] in a 3-D stacked NOC. Consider a multicast in a \( 4 \times 4 \times 4 \) mesh as shown in Fig. 3, which contains a 4 \( \times \) 4 sub-mesh in each layer as presented in Fig. 3. Two unicast packets can be delivered from \( v \) to \( w \), and \( z \) to \( w \) with disjoint link by using \( X-Y-Z \) routing in a 3-D mesh. Let us consider a 4 \( \times \) 4 \( \times \) 4 3-D mesh. The address sequence \( (0,1,0) \), \( (1,1,2) \), \( (1,2,2) \), \( (1,2,3) \), \( (2,1,3) \), \( (2,2,0) \), \( (3,2,1) \), \( (3,2,2) \), \( (v'_s) \) is a dimension-ordered chain of a 3-D mesh-based NOC.

Fig. 2 presents the multicast tree to deliver a test packet from the router connected to the ATE to all destinations with four unicast steps. The numbers at
the arrowed lines present the unicast steps. Unlike the method in [34], we assume that the NOC is designed based on the channel overlap routing scheme [34]. Therefore, a test packet is delivered to the destination based on the channel overlap [35] routing scheme instead of dimension-order routing. The proposed method is suitable for NOCs designed by any other routing schemes.

We next enumerate the differences between the new unicast-based multicast scheme and the one proposed in [34]. The main differences are as follows: (1) A thermal-aware test scheduling scheme is proposed to avoid hotspots in the process of testing; (2) A new DFT architecture is proposed to control the new thermal-aware test scheme. (3) The response packet for each test packet is not sent back to the ATE immediately like the method in [34], but the final compacted responses in the MISR inserted into each core is delivered back to the ATE after all tests have been applied to the core. (4) The channel overlap routing scheme is used to deliver test packets in each unicast step in order to conform to the baseline routing of the NOC, which provides much more routing flexibility than the dimension-order routing scheme used in [7], [8], [34].

An MISR is inserted into each router, therefore, the synchronization for each unicast step is not necessary because our method only delivers the final compacted responses back to the ATE. Link contention is also no longer an issue because of the virtual channel router design and the MISR-based test response collection scheme. The reason why we arrange the destinations of the multicast operation into a dimension-order chain is that we still need to reduce the amount of link contention.

The pseudo-code of the unicast-based multicast scheme is presented in Figs. 1-2. The test packet is delivered to a node $c$ from the node connected to the ATE. The cores that have at least one fault covered by the test vector are arranged into a dimension-ordered chain $D$. The core sequence is divided into two equal parts $D_1$ and $D_2$. Let $c$ be in the lower part $D_1$; it delivers the test packet to the first node $c_2$ in the upper half $D_2$, where $c_2$ will be responsible for the test packet delivery to all other cores in the $D_2$ using the same procedure recursively, and $c$ manages test packet delivery of the first part. If the core $c$ is in the upper part $D_2$, then it sends the packet to the last node $c_1$ in the first part $D_1$. The core $c_1$ manages test packet delivery for $D_1$, and the core $c$ still needs to handle test packet delivery of the second part recursively. Our method needs $\log_2 N + 1$ unicast steps to deliver a test packet to all destinations, where $N$ is the number of destinations related to the multicast operation.

As shown in Fig. 2, a test packet is sent to $v_i'$ ($1 \leq i \leq 8$), where all destinations and the source connected to the ATE are arranged as a dimension-ordered chain although the channel overlap instead of dimension-order routing is used in each unicast step. Fig. 2 shows that the

**Algorithm 1 NOC-testing()**

**Input:**
- The test packet set;

**Output:**
- Keep the test responses at the MISRs of cores;

1: while the test set is not empty do
2: for an unprocessed test vector $v$ do
3: Sort the cores detected by $v$ in the 3-D NOC into a dimension-ordered chain $D$. Delete $v$ from the test set.
4: Call $\text{deliver}(c, D)$ to deliver the test packet from the router connected to the ATE to any core $c$ in the dimension-ordered chain $D$.
5: end for
6: end while

**Algorithm 2 deliver(c,D)**

**Input:**
- Coordinates of the current node $c$ and the destination $D$;

**Output:**
- Delivery of the packet to $D$;

1: if $|D| = 2$ then
2: Deliver the packet to the remaining node;
3: else
4: divide $D$ into two equal subsets $D_1$ and $D_2$.
5: end if
6: if $c$ is in the lower half $D_1$ then
7: deliver the test packet from $c$ to the first node $c_2$ in the upper half $D_2$;
8: call $\text{deliver}(c_2, D_2)$ at $c_2$, call $\text{deliver}(c, D_1)$ at $c$.
9: end if
10: if $c$ is in the upper half $D_2$ then
11: deliver the packet from $c$ to the last node $c_1$ in the lower half $D_1$;
12: call $\text{deliver}(c_1, D_1)$ at $c_1$, call $\text{deliver}(c, D_2)$ at $c$.
13: end if
ATE is in the middle of the dimension-ordered chain. It can be at any location of the dimension-ordered chain.

The proposed unicast-based multicast scheme completes a multicast with multiple unicast steps, which is different from the original unicast-based multicast scheme [22]. The multicast source involves in all unicast steps in the original unicast-based multicast scheme [22]. Therefore, the ATE can deliver the second test packet in the second unicast step. The ATE delivers the test packet to node \( v_5 \) in the first unicast step as shown in Fig. 2, which is forwarded to node \( v_4 \) in the second unicast step as presented in Fig. 3(a). The test packet at \( v_4 \) is delivered recursively to \( v_1 \) while the packet at \( v_5 \) is delivered recursively to \( v_6 \) in the following two unicast steps.

As shown in Figs. 2 and 3, the test packet is delivered from the ATE to \( v_5 \), that is \((2,1,3)\) in the virtual network \( x+y+z^* \), in the first unicast step. The test packet received by \( v_4 \) is delivered to \( v_2 \) and \( v_1 \) in the second and the third unicast steps, respectively. The test packet is delivered in the virtual network \( x-y^*-z^* \) from \( v_4 \) to \( v_3 \) in the second unicast step. The test packet at \( v_2 \) is delivered in the virtual network \( x+y+z^* \) to \( v_1 \) in the third unicast step. In this way, the test packet finally reaches all destinations in four unicast steps. The proposed method reduces to a unicast problem when a test packet has a single destination. The test packet is delivered to the destination from the ATE by using the channel overlap routing scheme.

The proposed unicast-based multicast scheme as presented in Fig. 2 is different from the one in [22] and the method in [34] as shown in Fig. 3, where the numbers attached to the arrowed links are unicast step numbers. The ATE sends the test packet to any one of the destinations in the first unicast step based on the channel overlap routing scheme. It is shown that the source, that is connected to the ATE, involves in the multicast only in the first unicast step as shown in Figs. 2 and 3, but the source must be involved in all four unicast steps according to the unicast-based multicast scheme in [22]. In unicast step 3, the test packet is delivered from \( v_4 \) to \( v_2 \) along the given path.

Four unicast steps are sufficient to deliver the test packet to all eight cores. The proposed method can significantly reduce test delivery cost compared to the previous methods [7], [8] because the amount of test data required to be delivered from the ATE is greatly reduced. Test delivery time can also be reduced compared to the method in [34]. Figs. 3(a), (b), (c), and (d) present the details of four unicast steps using the unicast-based multicast scheme.

The multicast tree is kept in the header flits as the unicast-based multicast scheme in [22], which is implemented by just forwarding the dimension-ordered chain to the root of the multicast tree. Each core, that receives the test packet in the previous unicast step, determines its successors by running the procedure presented in Algorithms 1 and 2. A subset of destinations ordered into a dimension-ordered chain is forwarded to the corresponding successors. The process continues until all destinations have received the test packet.

### 3.2 Thermal-Aware Test Scheduling

Heat dissipation is an important issue for 3-D stacked NOCs. Peak temperature is closely related to the power consumption at a specific router and the corresponding core in the whole process of testing. We propose a thermal-aware test delivery scheme. A new test packet ordering scheme is proposed by avoiding the delivery of test packets to the hotspots to reduce the peak temperature in the NOC. The routing scheme to avoid hotspots is similar to a fault-tolerant routing scheme. An effective low-power scan testing scheme is necessary because power consumption for core testing contributes most to the power consumption at a node (including a router and a core) [7], [34]. The details of the low-power scan testing scheme is presented in Section 4.

The thermal-aware test scheduling procedure avoids delivering a test packet to the hotspots. Our method delivers the test packet to the hotspot cores when those
cores are not hotspots any more. The new method partitions the test process into multiple phases. The thermal information of the NOC is updated by HotSpot [15] after each test phase has been completed. Moreover, sensors on the chip can be integrated in the NOC in order to obtain the real-time thermal information, which can be used to guide thermal-aware test delivery.

The procedure for thermal-aware test scheduling is given in Algorithm 3. It provides a sequence of test packets for delivery. The current packet $p$ is selected when the delivery of $p$ does not violate the power constraint. Usually, the proposed method delivers packets to the same subset of cores for a number of consecutive test packets like [8], which can reduce the total power consumption of the NOC.

For a NOC with multiple different classes of cores, our method activates only one class of cores each time. The proposed low-power scan testing scheme also activates a small number of scan flip-flops for any scan shift cycles. Therefore, the proposed method does not need to evaluate whether the power constraint can be satisfied, unlike in [7], [8].

### 3.3 Unicast-Based Broadcast

The number of unicast steps is $\log_2 N + 1$ for the proposed unicast-based multicast scheme, where $N$ is the number of cores related to the multicast operation. The test delivery time and power consumption can still be very large when the NOC contains a single class of cores. A unicast-based broadcast scheme is proposed to deliver test packets in this case. The number of unicast steps can be reduced to three based on the new unicast-based broadcast scheme.

Fig. 4 presents the broadcast scheme with three unicast steps. The test packets from the ATE are delivered to all nodes in the leftmost column in layer 4 in the first unicast step as shown in Fig. 4(a). All other nodes in layer 4 except the core connected to the ATE receive the test packet in the second unicast steps as given in Fig. 4(b). Finally, all nodes in layer 4 deliver the test packet to all nodes in other layers in the third unicast step as shown in Fig. 4(c). The node $v$ right to the node that is connected to the ATE in layer 4 delivers the test packet to all nodes except the one connected to the ATE in the third unicast step. In the third unicast step, the test packets are delivered in the virtual network $x - y^*z -$ or $x - y^*z +$.

The test packet is not delivered to the hotspots. The test packets can avoid the hotspots as in fault-tolerant routing to avoid faulty nodes [35]. However, the technique to avoid hotspots can complicate test-packet delivery. Our method delivers all test packets across the hotspots, but does not deliver the packets to the corresponding cores. This scheme can significantly simplify the problem although some power consumption can be introduced at the routers of the hotspots. The power consumption at the cores during testing contributes much more to the total power consumption at a node [7].

### 4 Low-Power Scan Testing with Compressed Test Data

The power consumption of a NOC includes system-level power consumption in the NOC, and the power consumption inside cores for scan testing. The temperature increment is determined by the total power consumption produced during the period. Usually, the power consumption for scan testing inside cores contributes the most. We propose a new low-power scan testing scheme with compressed test stimulus data and compacted test response data. It uses a MISR-based unknown tolerant test response compactor. Therefore, the test data required delivering in the network can be further reduced compared to that in [36]. It is necessary to insert a decompressor into each core, however, the area overhead for the decompressor is very small.

Only a subset of scan flip-flops are activated in any shift clock cycle. The low-power scan testing scheme can provide low test application cost at the level of multiple scan chains. The benefits of compression test data lie not only in reducing test delivery time, but also in reducing power consumption and peak temperature. Subsection 4.3 presents the control logic to implement the proposed unicast-based multicast scheme.

#### 4.1 Scan Architecture to Tolerate Unknowns

The test responses may contain many unknowns for a real NOC system. The MISR-based compactor must avoid unknowns. The unknown responses may originate from uninitialized memory elements, floating bus...
Fig. 4. The unicast-based broadcast test delivery scheme: (a) the first unicast step, (b) the second unicast step, (c) the third unicast step, and (d) the whole broadcast.


drivers, false and multi-cycle paths and other sources that are found in real designs. Unlike the method in [34], the new method uses an MISR for each core to compact test responses. The MISR is established to be X-tolerant, which is independent of the test set. The new MISR-based X-tolerant test response compactor is completely different from the test-dependent one in [37].

Our method clusters the potential unknown sources into the same scan chains to tolerate unknown responses. Heuristics can be used when grouping scan flip-flops. For example, each group contains at most one scan flip-flop that produces unknowns. Scan flip-flops in each scan chain are driven by the same clock signal. Let \((C_1, C_2, \ldots, C_g)\) be the scan chains in the scan tree, and \(V\) be the test set. Our method selects another group \(G_1\) of scan flip-flops \((c_1', c_2', \ldots, c_g')\), which tries to connect the scan flip-flops \(c_1', c_2', \ldots, c_g'\) to any of \(C_1, C_2, \ldots, C_g\).

Suppose the new scan flip-flop group \(G_1 (c_1', c_2', \ldots, c_g')\) can be connected to the same scan tree. Let \(C_1, C_2, \ldots, C_g\) be the scan chains in the scan tree driven by the same scan-in pin. First, the potential unknown flip-flop is connected to the scan chain that produces unknowns. A scan flip-flop \(c_1' \in G_1\) is connected to a scan chain if the connection overhead is minimized. The above process continues until the scan tree has been constructed. All other scan trees can be established similarly.

A new technique is proposed to establish the test response compactor with unknowns after the scan trees have been constructed. Assume that each subset of scan chains are driven by a separate clock signal. We cluster scan chains, that produce unknown test responses, into the same XOR tree. Simultaneously, the new method also groups the scan flip-flops that simultaneously produce unknowns into the same scan chain subsets.

Any pair of scan chains \(C_1 (c_1, c_2, \ldots, c_d)\) and \(C_2 (c_1', c_2', \ldots, c_d')\) can be connected to the same XOR gate if the scan flip-flop pairs \((c_1, c_1'), (c_2, c_2'), \ldots, (c_d, c_d')\) do not have any common combinational predecessor.

The above process continues until the given number of scan chains have been selected or no scan chain can be connected to the XOR tree. A similar scheme is used to construct the second XOR tree. This procedure continues until all scan chains have been connected to the response compactor.

The scan-out pins, including the scan chains for the unknown sources, are all connected to the XOR trees for test response compaction. The scan-out pins of the clustered scan chains of the unknown sources are connected to the demultiplexers, whose outputs are connected another extra XOR tree. All the demultiplexers are controlled by an extra vector for each test vector, which indicates whether the test responses of the scan chain contain a unknown signal. Any scan chain that generates at least one unknown signal is masked by the MISR.

The ATPG tool is modified slightly by avoiding propagation of fault effects to the potential unknown sources. As mentioned earlier, the potential unknown sources are uninitialized memory elements, floating bus drivers, false and multi-cycle paths and other reasons that can be found in real designs. The outputs of the XOR trees are connected to the inputs of the MISR. Our method delivers the compacted final test responses in the MISRs back to the ATE. The time to deliver test response packets can be reduced significantly because the proposed method delivers at most a single response packet back to the ATE, and not one packet for each test vector. Moreover, the proposed unknown-tolerant MISR is independent of the test set.

4.2 Low-Power Test Application

The test generator can be modified to propagate fault effects away from the potential pseudo-primary outputs (PPOs) that capture unknown responses. The fault simulator is also be modified that the PPOs in the scan chains that are masked are set to unobservable. The modification of the test generator is trivial. Hence details are not presented here. Test delivery for X-tolerant test response packets is similar to that without unknown responses. Results for X-tolerant test and response delivery are presented in Section 6.

A gating technique unlike the one in [36] is used to reduce test power as shown in Fig. 5. The proposed method requires an extra vector for each test vector, which indicates whether the test responses of the scan chain contain a unknown signal. Any scan chain that generates at least one unknown signal is masked by the MISR. The ATPG tool is modified slightly by avoiding propagation of fault effects to the potential unknown sources. As mentioned earlier, the potential unknown sources are uninitialized memory elements, floating bus drivers, false and multi-cycle paths and other reasons that can be found in real designs. The outputs of the XOR trees are connected to the inputs of the MISR. Our method delivers the compacted final test responses in the MISRs back to the ATE. The time to deliver test response packets can be reduced significantly because the proposed method delivers at most a single response packet back to the ATE, and not one packet for each test vector. Moreover, the proposed unknown-tolerant MISR is independent of the test set.
size of the extra register. Each subset of scan chains is driven by a single clock signal. The scan chains driven by the same scan-in pin can be partitioned into multiple subsets, where each subset of scan chains is driven by the same clock signal from the extra register.

Our method inserts an extra multiplexer at the output of the AND gate for each clock signal. The selection signals of the multiplexers are the same as that for the scan chains. That is, the test clock signal \( \text{clk}_i \) ANDed with one of the signals \( R_1, R_2, \ldots, R_k \) drives each subset of scan chains when \( \text{test} = 1 \), and regular clock signal \( \text{clk} \) feeds to all scan chains when \( \text{test} = 0 \). Each bit of the extra register is connected to a hold latch, whose output is set to its input value during scan shift.

Only a subset of scan flip-flops is activated in any shift cycle. The low-power scan testing scheme provides test application cost is acceptable, which is close to that for the multiple scan chain design. The extra register is small in size. Compared to the method in [20], [36], the test data that must be delivered to a core is less because of the new test compression scheme, and the amount of test response data is also less. As shown in Fig. 5, \( O_1, O_2, \ldots, O_i \) are outputs of the test response compactor that may produce unknowns, which are not connected to the MISR.

The scheme to apply each test vector can be described as follows: (1) Activate a subset of scan chains, and disable all other scan chains; apply the test vector to the activated scan chains. (2) Continue the above process until the test vector has been applied to all scan chains. (3) All scan chains capture test responses.

The above simple test application scheme reduces shift power, but cannot reduce capture power. This restriction does not limit the thermal-aware test scheme in any significant way because the scan shift cycles contribute to most of power consumption [7], [34]. Only a subset of identical cores in the NOC is under test at any time in most cases if the NOC does not contain a single class of cores. If the NOC contains a single class of cores, the NOC can be partitioned into multiple subnetworks for low-power consumption consideration. A test packet is delivered to cores in a single subnetwork in any case.

Without loss of generality, the supply voltage \( V_{dd} \) is set to 1.5 V in this paper, and the functional frequency and test frequency are set to 1 GHz and 100 MHz, respectively. These parameters can be chosen appropriately in other scenarios. Capacitance for each gate is set to the fanout of each node for simplicity. The system-level power consumption is obtained by using Orion 2.0 [16], where capacitance data for all system-level components, such as switch, physical links, VC allocator, and switch allocator are obtained from the source tool.

4.3 Techniques to Control the Scan Testing Scheme in a NOC

The number of extra pins must be small enough. Each core requires a number of scan-in and scan-out pins, which can make the total number of extra pins large when the number of cores in the NOC is large. The number of test selection pins of the scan flip-flops for all cores can also be high if each core uses a separate test selection pin. Note that only cores of the same class can be tested concurrently.

All scan-in pins in a core are driven by the consumption buffer, therefore, no extra scan-in pins are necessary. All scan-out pins are connected to the MISR, where the output of the MISR is connected to the injection buffer. The injection buffer is the interface between the local node and the network, which injects packets to the network for the next unicast step or delivers the final response packet to the ATE. In our method, all cores share the same test selection pin as shown in Fig. 5. Therefore, the number of extra pins to control scan testing in a NOC is just one.

The extra pin \( x_1 \) that drives the extra register can also be shared by all cores, due to which another extra pin is necessary. An additional pin \( x \) is connected to all AND gates, which drive the scan chains directly. Each class of cores needs a separate extra pin \( x \). A global register can be added to the design, where each extra scan flip-flop of the global register is connected to the extra pins. It is not necessary to load the control vector (the value of \( x \)) for each test packet because the test packets are delivered to the same core subset in each test phase. That is, test packets are delivered to the same subset of destinations during the same phase.

The test packet is delivered to the core when \( x = 1 \). When \( x = 0 \), test delivery and test application have nothing to with the class of cores. The scan chains in the cores are disabled if \( x = 0 \). All scan chains are controlled by the signals from the extra register if \( x = 1 \). All core classes share in the same extra bit for control data delivery. Therefore, the size of the extra register to keep the control data for \( x \) is equal to the maximum number of cores for the same class.

Our method needs \( k \) extra pin \( c \) for all cores as shown in Fig. 5, where each extra pin drives a class of cores and \( k \) is the number of different classes of cores (\( k \) is set to no more than 4 in this paper). If \( c = 1 \), the class of cores is under test. However, the number of extra pins for \( c \) can be further reduced by using an extra register. In any case, there is only one of the extra pins set to value 1, and all other pins are set to 0.

The scan-in pins can be driven by a demultiplexer as shown in Fig. 5, and the input of the demultiplexer is the consumption channel. One of the output ports of the demultiplexer drives the scan-in pins, and the other is the channel connected to the processor to deliver operating packets. The selection pin of the demultiplexer is the output of the AND gate whose inputs are \( x \) and \( c \).

As for scan testing inside each core, our method partitions all scan trees into \( M \) subsets, where only one subset of scan trees is activated in a single cycle during the shift cycles. Power consumption inside the core can
be reduced to about $1/M$ in most cases compared to test power consumption of the test application scheme that applies a test to all scan chains simultaneously. However, test application time based on the low-power test application scheme increases about $M$ times compared to the scan forest architecture [38], but it is equal to that with the multiple scan chains.

All scan-out pins of the X-tolerant MISR are connected to the injection buffer at each core. The outputs $O_1, \ldots, O_7$ of the MISR are connected to the inputs of the injection port through a multiplexer, which is used to deliver the final test response in the MISR back to the ATE. Another input port of the multiplexer is the operating packets from the local processor. All multiplexers for all cores share the same extra pin $e$ as shown in Fig. 5. The injection port is the interface for each node from the core to the network. Outputs of the multiplexer do not need any extra pin. Connection between the output of the MISR is controlled by a single global extra pin via a multiplexer, whose another input is the injection channel.

5 Test-Response Collection

Test-response collection in [34] can be complex. As shown in Fig. 5, the test responses at a core is compacted by an MISR in the new method, where test responses of all test vectors are compacted into a single vector kept in the MISR. Test responses of the same class of cores are delivered back to the ATE as in the scheme presented in [34], which uses the reverse operation of the unicast-based multicast scheme. The successors of a node in the multicast tree to deliver the test packet become its predecessors in the test response, where the unique predecessor of each node in the multicast tree becomes its unique successor.

Test response packets do not contend for the resources of the NOC with the test packets because test responses are collected after all test packets have been delivered to all cores and applied to the cores. Test response packets for cores of the same class are delivered back to the node connected to the ATE as a single response packet. The test responses packets from different predecessors for response collection are compacted to a single packet by using bitwise XOR operation. The compacted test response packet is delivered to its unique successor in the test response collection graph as shown in Fig. 6. Therefore, each core in the dimension-ordered chain must keep its successors and unique predecessor in the multicast tree, which are presented as the predecessors and the unique successor in the response collection graph. The successors in the multicast tree are kept at each core for test packet delivery, and the unique predecessor is used for test response collection. The saved information for the dimension-ordered chain can be removed after the test packets for the same class of cores have been delivered. As shown in Fig. 6, all test response packets from the cores of the same class are delivered along the reverse paths in the multicast tree.

The scan-out pins are connected to the XOR trees for test-response compaction. The output of the test-response compactor is connected to the inputs of the MISR. The PPIs of the scan flip-flops at the same level of a scan tree can be assigned the same values for all test vectors, where the scan flip-flops must have no common combinational successor in the combinational part of the circuit for zero-aliasing response compaction. The test stimulus data can be compressed significantly and test responses can also be compacted considerably.

Synchronization of test response packets and stimulus data packets for the unicast-based multicast scheme can be a problem. The new method does not require us to synchronize test response or test stimulus data packets; the final response packet is simply transferred in the MISR for each core after all test packets have been delivered and applied to the core. There is only a single test-response packet for each core. It is therefore quite easy to implement delivery of the test-response packets even though the compacted response packets for different cores must be delivered separately.

Unlike the NOC testing scheme in [34], the new method inserts an extra MISR to each core. Therefore,
it is not necessary to deliver the test responses for each test packet. The time to deliver test response packets can be reduced significantly. Another important attribute of the proposed method is that it saves power consumption and reduces the test-response data volume delivered back to the ATE.

The amount of test-response data that must be transferred in the network can be significantly reduced compared to the technique to deliver the test-response packet separately for test packet inside each core [7], [8]. Compared to the method in [36], the amount of test response data that must be delivered is also much less. The test response data delivered back to the ATE can be reduced to only a few hundred of bits for NOC core testing. The test-response data volume for diagnosis is only a little more, but it is trivial compared to test stimulus data volume.

As shown in Fig. 5, test responses at a core are compacted to a single vector and kept in a MISR. Our method uses two different schemes to deliver the test responses back to the ATE for different purposes: (1) diagnosis, and (2) test. In the first case, the failing core can be identified, therefore, test responses of separate cores are delivered back to the ATE separately.

Let us consider the first case. Each core must deliver a separate test-response packet back to the ATE. Our method still uses the channel overlap deadlock-free adaptive routing scheme as presented in [36] to deliver test-response packets. The size (in bits) of the test-response packet is the same as the size of the MISR for response compaction, as shown in Fig. 5.

In the second case, test responses of the same class of cores are delivered back to the ATE. The scheme to deliver the test-response packets uses the reverse operation of the unicast-based multicast scheme. The leaf nodes of the multicast tree become the sources of the test response collection graph, while the root of the multicast tree (the node connected to the ATE) becomes the single sink. The final test response packet delivered to the sink node is sent back to the ATE.

Each core in the dimension-ordered chain must keep its predecessor where it receives the test packet. The predecessor in Fig. 3 is the successor in the test response collection graph, when all successors of a core in the multicast tree for test data delivery are its predecessors in the test-response collection graph as presented in Fig. 6. Consider the example shown in Fig. 6. The node $v'_2$ keeps the successor $v'_3$, and predecessors $v'_1$ and $v'_2$ as presented in the test response collection graph as presented in Fig. 6.

The above information is removed after the test-response packet has been delivered back to its predecessor in the unicast-based multicast tree (or the unique successor in the test-response collection graph as presented in Fig. 6). The test-response packets are compacted into a single packet for NOC core testing by a bitwise XOR operation after a core shown in Fig. 7(b) has received test-response packets from all its successors. Test-response compaction in this way does not need any hardware overhead, without incurring any coverage loss.

Let us illustrate the test-response collection scheme by using the example presented in Fig. 7. As shown in Fig. 7, test responses of the eight cores are compacted into a single packet and sent back to the ATE. Figs. 7(a), (b), (c), and (d) present paths for test response delivery in unicast Steps 1-4, respectively. It is required that the test-response packet at $v'_1$ be delivered to $v'_2$, the test response packet at $v'_2$ be forwarded to $v'_4$, and $v'_6$ to $v'_5$ in unicast Step 1 as presented in Fig. 7(a). The routing paths to deliver the test response packets in all unicast steps based on the channel overlap routing scheme are presented in Fig. 7(a). In particular, the response packet is delivered from $v'_5$ to the ATE inside the virtual network $x-y^*z-$ in the unicast Step 4.

### Table 1

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<th>FFs</th>
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<td>876</td>
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<td>ethernet</td>
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</table>

### Table 2

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<th>Xiang [34] (cyc)</th>
<th>proposed del(cyc)</th>
<th>area ppm CPU</th>
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</table>

6 **Experimental Results**

We have implemented the proposed method and the methods in [8] and [34]. Only single stuck-at faults are considered in this paper. Testing of NOC for transition faults can be carried out in a similar manner. We assume that test application is started immediately after a test packet has been received at each core. At most three packets can be kept at the injection buffer and the consumption buffer at each router in all experimental results in this paper. The consumption buffer is the interface between the network and the processor, and the injection buffer is the interface between the processor and the network.

The final test responses kept in an MISR are injected to the NOC from a core via the injection buffer and delivered back to the ATE, which is consumed at its successor in the test-response collection graph as shown in Fig. 6. The test-response packets consumed at the same core are compacted into a single test-response packet, which is injected into the NOC again and delivered to its unique successor in the test-response collection graph. The process continues until the test-response packet reaches the node connected to the ATE.
We have implemented the proposed method by using the three largest IWLS2005 circuits, i.e., ethernet, des_perf, vga_lcd, and the largest ITC99 circuit b19. Table 1 presents the statistics of the circuits used in all experimental results. For the low-power scan testing scheme, scan flip-flops of the circuits are partitioned into ten subsets. All selected benchmark circuits are randomly assigned to the cores in a 8×8 mesh, which is mapped to a 4×4×4 3-D mesh. For example, four different cores are assigned to all nodes in a 4×4×4 3-D mesh, where each node is randomly assigned one of the four circuits. However, the number of times that each circuit appears in the NOC is \(16 - d \leq N \leq 16 + d\), where \(d\) is set to 10\% (it is 2 in this case) of the average number 16. It is found according to experimental results that the number of different core classes has great impact on test cost, but the exact numbers of specific cores, locations of different cores have smaller influence. Therefore, all results are obtained according to a single core assignment.

In Table 2, area overhead (percentage) of the new method is presented in the column area. The CPU time (seconds) to estimate temperature of the proposed method is presented in column CPU based on the thermal analysis tool HotSpot [15]. Circuits b19, des, ethernet and vga are randomly inserted into the cores when the NOC contains four separate classes of cores. Circuits b19, des and vga are randomly assigned to all cores when the NOC contains three separate classes of cores. In a NOC that contains a single class of cores, circuit b19 is inserted into all cores.

Table 2 presents the test-delivery time (cycles) of the proposed method (del), the method in [34] and the method proposed by Cota [8] in the first three columns. The columns \(T_1\) and \(T_2\) present the test delivery time reduction of the proposed method compared to [8] and Xiang [34], respectively. The proposed method obtains up to 3297X and at least 1000X reduction in delivery time compared to the method in [8]. The proposed method is more effective when the number of core classes decreases as shown in Table 2, which also reduces the test delivery time for the proposed method. The reason is that only the first unicast step for each test packet contributes to the test time (ATE). The ATE delivers the next test packet after the first unicast step of a test packet. Any test packet is shared by more cores when the number of core classes decreases, therefore, the number of test packets decreases. The features of the cores can also have impact on the performance. Compared to the method in [34], the new method provides less improvement because both methods use unicast-based multicast schemes.

We use a combination of the scan forest and a coding-based test compression scheme (the selective coding scheme in the paper) for the new method to compress test data at each core. The coding-based test compression scheme does not compress test data well for circuits des and b19 as shown in Fig. 5 after the scan forest architecture has been applied. This is the reason why the test delivery time reduction for NOCs with three, and a single core classes does not proportionally decrease compared to [34].

We just use the method in [8] as a baseline method to compare. The reason why the proposed method is more effective for test delivery time is that: (1) the method in [8] does not consider identical cores; however, the proposed method uses a unicast-based multicast scheme like [34], while any test packet is shared by the cores that are identical; each test packet contributes just the first unicast step to ATE time like [34]; (2) a more effective test compression scheme is adopted, therefore, the amount of test data is less; (3) test responses are compacted by the new X-tolerant MISR-based compactor, due to which at most one test response packet is necessary for each core.

Table 3 presents the test data volume for the three methods. The coding-based scheme combined with scan forest [36] can further compress test data (test) effectively compared to [34] that used only a scan forest. Test response data (TR) is much less than both of the previous methods. The sizes of the MISRs for different cores b19, des, ethernet, and vga are set to 30, 30, 50, and 30, respectively, in the proposed method. The columns \(T_1\) and \(T_2\) in Table 3 presents the times of test data volume reduction of the proposed method compared to the methods in [8] and [34].

Test data and test response data of different cores must be delivered separately based on the method in [8] and [34]. However, the new method only requires delivering the final compressed test response in the MISRs. Test response packets can lead to waste of bandwidths and introduce high power consumption, which can increase the peak temperature.

The test data are transferred to the core connected to the ATE first. They are established into packets and

<table>
<thead>
<tr>
<th>core</th>
<th>Cota [8]</th>
<th>Xiang [34]</th>
<th>proposed</th>
</tr>
</thead>
<tbody>
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Fig. 8. Performance of the thermal-aware test scheduling scheme in a NOC with four different classes of cores.
multicast to all related cores. We assume that each physical channel has two virtual channels in the 3-D stacked NOC. The start-up and receipt latency are included, which are set to ten clock cycles in all simulation results. The consumption buffer for each core can keep up to three test packets, while the injection buffer provides enough buffer to keep three packets. Two adjacent routers transfer a single flit data for each clock cycle, where a flit contains 32 bit data.

Power consumption of the cores and the NOC (including power generated by the channels and the routers, estimated by Orion 2.0 [16]) is considered together. The total power consumption in the NOC during test application can be mainly attributed to the power consumed during core testing. Test packet delivery contributes much less power consumption. We adopt a low-power core testing scheme to reduce test power. This scheme can greatly relax the test-power constraint and boost parallelism for test data delivery. Results show that the proposed thermal-aware scheduling scheme still outperforms the previous methods.

Figs. 8-10 present the peak temperature introduced by the test procedure in a 3-D stacked NOC. Fig. 8 presents peak temperature information of a NOC with four different classes of cores. It is found that the proposed method obtains more than a 20°C reduction compared to the method in [8], and an apparent peak temperature reduction compared to the method in [34].

Fig. 9 presents peak temperature reduction for a NOC with three different classes of cores. The proposed method obtains more than 20°C peak temperature reduction compared to [8]. In the process of test delivery, the proposed method obtains up to 40°C peak temperature reduction compared to [8].

Fig. 10 presents the performance comparison of the new method with both previous methods when the NOC contains a single class of cores (b19). Again, the new method obtains much lower peak temperature than that produced by [8]. The new method also leads to lower peak temperature than the method in [34] in all cases according to the final peak temperature after all tests have been applied as presented in Figs. 8, 9, and 10 mainly because the new method delivers less stimulus test data and leads to a negligible amount of test response data. The method in [34] and the new method adopt a similar low-power test application scheme.

7 CONCLUSIONS

Three-dimensional (3-D) stacked network-on-chip (NOC) designs constitute an important emerging technology. Unbalanced heat dissipation in 3-D stacked NOCs introduces hotspots, especially, when a large amount of test data must be applied for quality assurance. We have presented a thermal-aware test scheduling scheme to reduce peak temperature produced by testing. Thermal-aware test scheduling avoids delivering test packets to hotspots in the NOC with a new unicast-based multicast scheme by making full use of the homogeneity of the cores in the NOC. Test responses are compacted on-chip by an unknown-tolerant MISR at each node. Test data are applied to cores by using a low-power test application scheme. It is shown that the proposed method can significantly reduce the peak temperature, test time, and test data volume compared to previous methods [8], [34]. The authors would like to express their thanks to Gang Liu for his preparation of the experimental results presented in this paper.

REFERENCES


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