Enhanced LCCG: A Novel Test Clock Generation Scheme for Faster-than-at-Speed Delay Testing

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Abstract—On-chip faster-than-at-speed delay testing provides a promising way for small delay defect detection. However, the frequency of on-chip generated test clock would be impacted by process variations. Hence, it requires determining the actual frequency of generated test clock to ensure the effectiveness of faster-than-at-speed delay testing. In this paper, we present a novel test clock generation scheme, namely Enhanced LCCG, for faster-than-at-speed delay testing. In the proposed scheme, faster-than-at-speed test clock is firstly generated by configuring the corresponding control information specified in the test pattern into Enhanced LCCG. Then, by constructing oscillation paths and counting the corresponding oscillation iteration numbers, the actual frequency of test clock can be measured and calculated with high resolution. Experimental results are presented to validate the proposed method.

Keywords—faster-than-at-speed; delay testing; small delay defect;

I. INTRODUCTION

With the semiconductor process technology shrinking to smaller size, manufacturing process-related defects, such as resistive opens and shorts, gate oxide failures, via voids, etc., are becoming more and more prevalent in modern integrated circuits [1, 2]. The probability of timing-related failures caused by these defects is then reaching a remarkable value. Therefore, in order to ensure the quality of shippable products, it is imperative to test timing-related failures [3]. At-speed delay testing is typically adopted for timing related defect detection by checking whether the circuit under test (CUT) meets the specified clock frequency or not. However, the at-speed delay testing method has a weak ability for detecting small delay defects (SDD), since the small delay defect introduces only a small extra delay over its normal value and could easily escape detection when the test slack is large.

It is well known that small delay defects pose a serious threat to the chip’s quality and reliability [4, 5]. For instance, if a resistive open defect with only a small extra delay that escapes the at-speed delay testing detection is activated on a critical path during functional application, then a timing failure will occur in the field. Moreover, even if the resistive open defect hidden in the circuit wouldn’t cause a timing failure during functional application, it is prone to degrade during the subsequent operations and will become a complete open. As a result, it is an imperative requirement to provide effective methods to detect small delay defects for ensuring the quality and reliability of modern integrated chips.

In recent years, many researches have been attracted by the faster-than-at-speed delay testing method, for it can provide an effective way for small delay defect detection. The faster-than-at-speed delay testing method is implemented by using test clocks with frequencies faster than that of functional clock. Clearly, by increasing the frequency of test clock, the slack of circuit path under test will be reduced, thereby increasing the probability of small delay defect detection. However, it is very costly to use external automatic test equipment (ATE) to provide high speed test clocks. Moreover, even without considering the high cost, the effectiveness of faster-than-at-speed delay testing with test clocks provided by ATE will still be limited due to the reason that the frequency of test clock generated by ATE would be affected by factors such as parasitic capacitance, resistance of probe, tester skew, etc.[6] Therefore, it requires generating faster-than-at-speed test clock on chip to exert the advantage of faster-than-at-speed delay testing.

A. Previous Work

Several on-chip faster-than-at-speed delay testing methods have been proposed in literatures. In [7], a clock control architecture is proposed for supporting on-chip faster-than-at-speed delay testing, in which the PLL is adopted. However, it would be time consuming by adopting this method for faster-than-at-speed delay testing, since the PLL need to be reset before applying each test pattern. In [8], by designing an in-situ delay clock generator and a pulse programmable selection generator, high speed test clock can be provided for faster-than-at-speed delay testing. However, it can only be used for launch on capture (LOC) test framework, and consumes a relatively large hardware overhead. Moreover, the maximum frequency of generated test clock is strictly limited. In [9], an on-chip programmable capture generator (PCG) circuit is proposed and can be used to provide high speed test clock for faster-than-at-speed delay testing. However, the faster-than-at-speed delay testing architecture adopting PCG should be exclusively designed to support launch on capture (LOC), launch on shift (LOS), and enhanced scan (ES) test frameworks, respectively. In [10], an on-chip launch and capture clock generation circuit (LCCG) for faster-than-at-speed delay testing is proposed. The LCCG includes multiple delay control stages and can be incorporated into anywhere of the scan chain. Depending on the delay difference of each delay stage, the test clock can be generated with expected frequency by specifying the frequency control information in the test pattern to configure the delay control stages of LCCG.
Similarly, the test frameworks and clock signals selection can also be configured by specifying the corresponding control information in the test patterns. The faster-than-at-speed delay testing architecture using the proposed LCCG circuit is also proposed in [10], which can support both LOC and LOS delay testing frameworks.

By designing LCCG, the test clock can be easily generated with programmable frequency for faster-than-at-speed delay testing. The hardware overhead of LCCG is also very low. However, there are two problems that possibly occur in LCCG:

1. The frequency of test clock relies on the delay differences of the specified delay stages. Clearly, if delay defects occurred in the path for generating test clocks in LCCG, then the frequencies of generated test clocks would be severely deviated from the expected values.

2. As the process variations in modern integrated circuits are very prominent [14, 15], the delay differences of the delay stages are thus unavoidable to suffer from variations. Therefore, the frequencies of generated test clocks would also be severely deviated from the expected values.

Consequently, the actual frequencies of the test clocks generated by LCCG cannot be exactly ascertained during the faster-than-at-speed delay testing caused by the above two reasons. If the actual frequencies of test clocks are still treated as expected values, the effectiveness of faster-than-at-speed delay testing would be impacted. For instance, if the actual frequency of test clock is larger than the expected value, yield loss may be caused due to the excess frequency. In contrast, if the actual frequency of test clock is smaller than the expected value, small delay defects may still be hidden in the chip. However, the real scenario of small delay defect detection can hardly be figured out because of unknowing the actual frequencies of test clocks.

B. Contribution and Paper Organization

In this paper, an enhanced launch and capture clock generation circuit (Enhanced LCCG) is presented, which inherits the advantages and conquers the drawbacks of the original LCCG. In the proposed scheme, faster-than-at-speed test clock is firstly generated by configuring the corresponding control information specified in the test patterns into Enhanced LCCG. Then, by constructing oscillation paths and counting the corresponding oscillation iteration numbers, the actual frequency of test clock can be measured and calculated with high resolution. Therefore, in the faster-than-at-speed delay testing, the actual frequencies of all generated test clocks by Enhanced LCCG can be measured firstly, and then the test clock, of which the actual frequency has the best approximation to the expected value, can be chosen for faster-than-at-speed delay testing.

The remainder of the paper is organized as follows. Section II describes the proposed Enhanced LCCG, which can be used for faster-than-at-speed delay testing. The experimental results are presented in Section III. Section IV concludes the paper.

II. THE PROPOSED FASTER-THAN-AT-SPEED DELAY TESTING WITH ENHANCED LCCG

In this section, we proposed an enhanced launch and capture clock generation circuit, called Enhanced LCCG, by which the test clock can be generated with known frequency for supporting effective faster-than-at-speed delay testing. The key idea of the proposed Enhanced LCCG is to measure the actual frequency of test clock based on oscillation technique before the application of the generated test clock for faster-than-at-speed delay testing. In the following subsections, the faster-than-at-speed delay testing clock generation method will be presented firstly, and then the method for determining the actual frequencies of generated test clocks will be described.

A. The Generation of Faster-than-at-Speed Test Clock

The basic architecture of the proposed Enhanced LCCG is presented in Figure 1, which consists of multiple delay control stages, an oscillation controller, and an n-bit counter, etc. Similar to the original LCCG [10], the delay control stages included in Enhanced LCCG are also used to configure the frequency of test clock. The delay units in each delay stage are named upper delay unit (UDU) and lower delays (LDU) respectively. The delay of LDU is designed larger than that of UDU. Clearly, the main purpose of the delay control stage is to adjust the delay difference of output signals for each delay stage. The delay difference between LDU and UDU is considered to be the delay range of the corresponding delay stage.

It can also be noted from Figure 1 that there are four multiplexers designed in Enhanced LCCG, where the selection signals are C1', C2', C3 respectively. The C1' and C2' signals are generated by the oscillation controller, which is shown in Figure1 and redrew in Figure 2 in detail. The main purpose of the four multiplexers is to configure the operation mode of Enhanced LCCG. The operation modes of Enhanced LCCG consist of test clock generation mode and oscillation mode. There also exists a rising-edge-triggered n-bit counter in Enhanced LCCG, which is used to count the oscillation iteration number under the oscillation mode of Enhanced LCCG, and will be described in detail in the next subsection.

Suppose C1, C2, C3, C4, and Ostart signals are initialized to logic high, high, low, low, and high values, then Enhanced LCCG would be configured to test clock generation mode. Since C4 is low, the C1 and C2 will be sent to C1' and C2' through multiplexers. The states of D-type flip-flops in the delay stages can also be initialized to the required logic values during the scan-in cycles.

Figure 3 illustrated the timing waveform of critical signals in Enhanced LCCG for faster-than-at-speed test clock generation. It is known that the global scan enable (GSEN) signal keeps logic high value when the test patterns are scanned into the scan chain [12]. As described in [12], the GSEN signal would switch to logic low value after the last scan-in cycle for supporting both LOC and LOS delay testing.
frameworks. As shown in Figure 3, depending on the state of D-type flip-flop in each delay stage, rising transitions will be generated at LAUCLK and CAPCLK with specified delay difference after the GSEN signal switched to logic low value.

Clearly, since C1 and C2 are initialized to logic high values, the test clock TCLK, in which the launch and capture edges are derived from LAUCLK and CAPCLK signals, can then be generated by using OR gate for faster-than-at-speed delay testing. The respective delays of LAUCLK and CAPCLK to the corresponding input of OR gate can be designed basically equal \[10\]. The impact of OR gate to the frequency of TCLK is ignored. Ideally, the frequency of TCLK would be completely determined by the delay ranges and the control values of delay stages. However, as mentioned before, the actual frequencies of generated test clocks may be severely deviated from the expected values due to process variations and the possible occurrence of delay defects in Enhanced LCCG. Hence, it can hardly know the real effectiveness of small delay defect detection due to the deviations of test clock frequencies.

Consequently, in order to ensure the effectiveness of faster-than-at-speed delay testing, it is imperative to measure all the actual frequencies of generated test clocks before the application of them for faster-than-at-speed delay testing. The test clock sets, in which the measured frequency has the best approximation to the frequency to be applied, can be chosen for faster-than-at-speed delay testing. The way for measuring the actual frequencies of test clocks is described in the next subsection.

B. The Measurement of Actual Frequency of Test Clock for Effective Faster-than-at-Speed Delay Testing

It is very important to note from Figure 1 and Figure 3 that the actual period of test clock is in fact equal to the delay difference between \[\uparrow\text{Path1} \rightarrow \text{Path2}\] and \[\uparrow\text{Path1} \rightarrow \text{Path2}\], where the arrow specifies the transition direction at the input of the path. It is
known that the ring oscillator based architecture provides an effective approach for ring path delay measurement [13]. Hence, in this work, we propose to measure the delay difference between Path1 and Path2 by using oscillation technique, thereby obtaining the actual frequencies of test clocks for effective faster-than-at-speed delay testing. Obviously, the critical question for measuring the delay difference between Path1 and Path2 is how to construct the oscillators and then to calculate the delay differences.

In Enhanced LCCG, we propose to design Path3, multiple multiplexers, an oscillation controller, etc., for configuring the Path1 or Path2 into oscillators, as shown in Figure 1. In fact, the key idea of the proposed method is to firstly obtain the path delay of Path1, Path2, Path3, and Path1 + Path2 + Path3 - Path1 - Path3 by oscillation, respectively, and then to obtain the delay difference between Path1 and Path2 by subtracting the delay measurement result of Path2 - Path3 - Path1 - Path3 from that of Path1 - Path3 - Path1 - Path3.

In the following, the way for obtaining the delays of Path1, Path3, Path2, and Path1 - Path2 - Path3 - Path1 - Path3 will be presented in detail. The timing waveform of critical signals for measuring the delay of Path1, Path3, Path1 - Path2, and Path1 - Path3 by using oscillation technique is shown in the Figure 4.

![Figure 4. Timing Waveform of Enhanced LCCG](image)

Clearly, if the C1, C2, C3, and C4 are initialized to logic high, low, high, and low values respectively, Path1 - Path3 - Path1 - Path3 will be configured to an oscillator. Then a ring oscillation signal can be created in Path1 - Path3 - Path1 - Path3 by switching the Ostart signal from logic low to high value. Hence, the n-bit counter can get the oscillation iteration number in a given oscillation time. The delay of Path1 - Path3 - Path1 - Path3 can then be calculated as follows:

\[ \uparrow P1 + \downarrow P1 + \uparrow P3 + \downarrow P3 = \frac{T}{N} \] (1)

The \( \uparrow P1 \), \( \downarrow P1 \), \( \uparrow P3 \), and \( \downarrow P3 \) represent the delays of Path1, Path1, Path3, and Path3 respectively. The N represents the oscillation iteration number and the T represents the given oscillation time.

The control for configuring the Path2 - Path3 - Path1 - Path3 into an oscillator is more complex. In order to configure the Path2 - Path3 - Path1 - Path3 into an oscillator, the C1, C2, C3, and C4 should be set to don’t care, don’t care, high, and high values, respectively. Moreover, the rising-edge-triggered and falling-edge-triggered D-type flip-flops in oscillation controller should be initialized to logic low values by reset signal. Hence the C1’ and C2’ will also be initialized to logic low and high values respectively. When the Os_input signal is switched, the C1’ and C2’ will be inverted when the Os_input signal is switched. Therefore, a falling transition will be propagated through Path3, and then inverted to propagate through Path3. The control signals C1’ and C2’ will be inverted when the Os_input signal is switched. Consequently, Path2 - Path3 - Path1 - Path3 can be configured to an oscillator by using the oscillation controller.

Clearly, the delay of Path2 - Path3 - Path1 - Path3 can be calculated as follows:

\[ \uparrow P2 + \downarrow P1 + \uparrow P3 + \downarrow P3 = \frac{T}{M} \] (2)

where the \( \uparrow P2 \) represent the delay of Path2, the M represents the oscillation iteration number. Consequently, the delay difference between Path1 and Path2, which reflects the actual frequency of test clock, can be calculated by subtracting (2) from (1) and expressed as follows:

\[ \uparrow P1 - \downarrow P2 = \frac{\frac{T}{N}}{\frac{T}{M}} \] (3)

In order to achieve satisfactory delay measurement accuracy for Path1 - Path3 - Path1 - Path3 and Path2 - Path3 - Path1 - Path3 respectively, enough oscillation time should be estimated and given[13]. Suppose \( R_0 \) represents the desired delay measurement resolution for Path1 - Path3 - Path1 - Path3, then the oscillation time T and the oscillation iteration number N should be satisfied the following expression to achieve the desired resolution:

\[ \frac{\frac{T}{N}}{\frac{T}{N} + 1} = \frac{\frac{T}{N}}{\frac{T}{N} + 1} \leq R_0 \] (4)

In expression (4), \( \frac{T}{N} + 1 \) can be approximated to be an oscillation period and easily estimated by using timing analysis tools. Suppose \( \frac{T}{N} \) represents the estimated oscillation period for Path1 - Path3 - Path1 - Path3 by timing analysis, then the expression (4) can be transformed to:
The delay measurement resolution can be satisfied. The delay measurement resolution can be improved with the increase of oscillation time. The analysis method of delay measurement resolution for Path1- Path3, the minimum oscillation time $T$ as shown in (6) should be satisfied. The delay measurement resolution can be improved with the increase of oscillation time. The analysis method of delay measurement resolution for Path1- Path3, the minimum oscillation time $T$ as shown in (6) should be satisfied. The delay measurement resolution can be improved with the increase of oscillation time.

$$N_{\text{min}} \geq \frac{t_{\text{period}}}{R_2}$$  \hspace{1cm} (5)

$$T \geq N_{\text{min}} \times t_{\text{period}}$$  \hspace{1cm} (6)

Where $N_{\text{min}}$ represents the minimum required oscillation iteration number for ensuring the desired delay measurement resolution. Therefore, in order to ensure the desired delay measurement resolution for Path1- Path3, the minimum oscillation time $T$ as shown in (6) should be satisfied. The delay measurement resolution can be improved with the increase of oscillation time. The analysis method of delay measurement resolution for Path1- Path3 is also suitable for that of Path2- Path3.

III. EXPERIMENTAL RESULTS

The proposed Enhanced LCCG architecture, which supports effective faster-than-at-speed delay testing, was implemented using SMIC 0.18μm CMOS technology in this work. The experimental results consist of two main parts: 1) measured and simulated test clock periods for multiple test clock configurations; 2) measured and simulated test clock periods for a test clock configuration under process variations.

In the first experiment, six cases of test clock configuration are considered to verify the effectiveness of the proposed Enhanced LCCG in the test clock periods with expected frequencies by configuring the corresponding control information into Enhanced LCCG.

Table I shows the simulated and measured test clock periods for six test clock configurations, which are obtained by using HSPICE simulation. The column “Test Clock Configuration” represents the simulated test clock period under the corresponding test clock configuration without considering process variations. The column “Measured Period” represents the measured test clock period under the corresponding test clock configuration by using the proposed method, in which the oscillation time $T$ is set to 5000ns for the sake of saving simulation time with an acceptable resolution. The column “Absolute Error” represents the absolute value of error between “Measured Period” and “Simulated Period”, while the column “Relative Error” represents the ratio of “Absolute Error” to “Simulated Period”. Clearly, it can be noted from Table I that the errors between the measured and simulated periods are very small, which indicates that the proposed scheme can measure the actual frequencies of test clocks with high resolution. Moreover, as mentioned before, the delay measurement resolution will be improved with the increase of oscillation time.

![Figure 5](image-url)  
**Figure 5. Oscillation Iteration Number and Error Range**

Figure 5 shows the oscillation iteration numbers of Path1- Path3 for multiple test clock configurations and Path1- Path3 and Path2- Path3 for Path1- Path3 when measuring the periods of six test clocks as presented in Table I, which is obtained from the n-bit counter by HSPICE simulation. Based on the simulated oscillation iteration numbers, the maximum error for each period measurement can then be calculated, which is also shown in Figure 5.

Table I shows the simulated and measured test clock periods for six test clock configurations, which are obtained by using HSPICE simulation. The column “Test Clock Configuration” represents the simulated test clock period under the corresponding test clock configuration without considering process variations. The column “Measured Period” represents the measured test clock period under the corresponding test clock configuration by using the proposed method, in which the oscillation time $T$ is set to 5000ns for the sake of saving simulation time with an acceptable resolution. The column “Absolute Error” represents the absolute value of error between “Measured Period” and “Simulated Period”, while the column “Relative Error” represents the ratio of “Absolute Error” to “Simulated Period”. Clearly, it can be noted from Table I that the errors between the measured and simulated periods are very small, which indicates that the proposed scheme can measure the actual frequencies of test clocks with high resolution. Moreover, as mentioned before, the delay measurement resolution will be improved with the increase of oscillation time.

![Figure 6](image-url)  
**Figure 6. Measured and simulated test clock periods under process variations (30 Monte Carlo iterations)**

In order to validate the effectiveness of Enhanced LCCG, HSPICE Monte Carlo simulations with 30 iterations are conducted. In the Monte Carlo simulations, both inter-die and intra-die process variations are considered. The inter-die and intra-die gate length variations are considered to have Gaussian distributions, $N(\mu_1, \sigma_1)$ and $N(\mu_2, \sigma_2)$, respectively [5,11,13,14,15]. The $\sigma_1$ and $\sigma_2$ represent the standard deviations of gate length for inter-die and intra-die variations respectively. The $\mu_1$ represents the typical transistor channel length. The
variations considered in the Monte Carlo simulations are $3\sigma_1=0.15\mu_A$ and $3\sigma_2=0.15\mu_A$. Figure 6 shows the simulated and measured test clock periods for test clock configuration of Case1 under the above assumed process variations. It can be noted from Figure 6 that the test clock periods obtained from simulation and measurement by using the proposed Enhanced LCCG are very close. The maximum absolute error between measurement and simulation is only about 16ps, which can still be further reduced by increasing the oscillation time. Consequently, by using the proposed Enhanced LCCG, the actual frequencies of generated test clocks can be obtained with high resolution, thereby realizing effective faster-than-at-speed delay testing.

IV. CONCLUSIONS

In this paper, we have proposed a novel launch and capture clock generation scheme, namely Enhanced LCCG, for faster-than-at-speed delay testing. In the proposed scheme, faster-than-at-speed test clock is firstly generated by configuring the corresponding control information specified in the test patterns into Enhanced LCCG. Then, by constructing oscillation paths and counting the corresponding oscillation iteration numbers, the actual frequency of test clock can be measured and calculated. Experimental results show that the proposed Enhanced LCCG can obtain the actual frequencies of test clocks with high resolution. Therefore, by obtaining the actual frequencies of test clocks firstly and then choosing the test clock with best approximation frequency to the expected value, effective faster-than-at-speed delay testing can be realized.

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