The Real-Time R-wave Detection
Based on FPGA

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Abstract—R-wave detection is one of the most significant parts in Electrocardiogram (ECG) signal studies and plays an important role in the automatic ECG analysis system. In this research, we design a prototype of portable automatic ECG analysis system based on field programmable gate array (FPGA) using Altera DE2-70 development board. The system includes four parts: 1) Data input, 2) ECG denoising, 3) ECG analysis and R-wave detection, 4) Results display. In this paper, we use the data from the well-known MIT/BIH arrhythmia database. CDF9/7 wavelet filter is used to remove the high-frequency noise and the threshold method is used to detect the R-wave. In addition, In the Quartus II 9.0 development environment, we complete the simulation and synthesis. Experimental results based on the system show that proposed architecture can detect R-wave accurately and the utilization percent of resource is low, just 6%.

Keywords—ECG, R-wave detection, CDF9/7 wavelet filter, Threshold, FPGA.

I. INTRODUCTION

Electrocardiogram (ECG) signal is one of the earliest biological signals studied and applied to clinical medicine. At present, ECG analysis is still one of the simplest noninvasive diagnostic methods for heart and cardiovascular disease. With the rapid development of electronic science technology and family medicine, the computer aided diagnosis system and portable ECG monitoring devices are developed, which make the ECG automatic analysis become a research focus in the field of Biomedical Engineering. However, automated analysis of ECG beats is a challenging problem because the morphological and temporal characteristics of ECG signals show significant variation for different patients under different physical conditions [1].

It is important that the reliable and accurate detection algorithm of the basic characteristic features of the signal for the automatic ECG analysis system. QRS wave is the most important part in ECG signal and used as the reference point for beat alignment. In recent years, there have been a lot of R-wave detection algorithms proposed, such as difference threshold value algorithm [2] [3], wavelet transform algorithm [4] [5] [6], template matching algorithm [7], neural network algorithm [8] [9], and others that combine the basic algorithms above [10] [11]. However, most of these algorithms are in the stage of theoretical research and processed offline. The studies of the hardware implementation of the algorithm are relatively small.

Nowadays, Field Programmable Gate Array (FPGA) is at the forefront of digital signal processing technology. We generally use the hardware description language, VerilogHDL or VHDL, to configure the FPGA. FPGA allows designers to add some new circuits, or reconfigure the hardware resources for the special functions even after the program has been downloaded into chips. The fast growing speed and circuit density of FPGAs have made them a significant player in domains earlier dominated by Application Specific Integrated Circuits (ASIC). Besides being used for general purpose logic design, modern FPGAs are equipped with building blocks for specialized applications such as DSP and embedded system design [12]. In recent years, FPGA has also been widely used in the field of ECG signal processing, such as ECG denoising system [13] [18], QRS wave detection [12] [14] and feature extraction. In [15], an accurate FPGA based ECG Analysis system is described. That design is based on popular software based QRS detection.

Our previous research [16] succeeded making lots of simulations for the real-time R-wave detection using CDF9/7 wavelet filter and difference method. In this paper, we try to implement them on a prototype of portable automatic ECG analysis system based on FPGA using Altera DE2-70 development board. FPGA system has high speed and the plentiful leaving resources, which make other more circuits can be easily join this design to form a larger system that has more functions. Moreover, at present, the researches for portable ECG device tend to be small size, low power and real-time data processing. So the portable ECG devices based on FPGA have a great advantage.

This paper is organized as follows. In section II, we describe the algorithm used in this system. This algorithm is our previous research, so we introduce the algorithm implementation process briefly and some improved places for more suitable for FPGA implementation. Section III introduces the design and implementation of ECG analysis system on FPGA. It is the most important part of our paper. We use MIT/BIH Arrhythmia Database to test system and give the data analysis and comparison in Section IV. Finally, the conclusions are made in section V.
II. ALGORITHM DESCRIPTION

In order to make the reader get a clearer understanding of our work, we introduce the process of algorithm compactly in our design. Fig.1 shows the process of algorithm in our design.

![Diagram showing the process of algorithm](image)

Fig.1 the process of algorithm in our design

At first, the CDF9/7 wavelet filter’s function is noise rejection. CDF9/7 wavelet is a lifting wavelet transform proposed by Sweldens [17]. Lifting wavelet transform is a new method of DWT, which needs less computation and smaller space of storage compared with the traditional wavelet filtering based on convolution. Besides, it is more suitable for hardware implementation. In the paper, CDF9/7 wavelet transform based on the lifting method is constructed as follows.

\[
\begin{align*}
S^{(o)}_i &= x_{2i} \\
D^{(o)}_i &= x_{2i+1} \\
D^{(2)}_i &= d^{(1)}_i + \alpha s^{(1)}_i + \alpha s^{(1)}_{i+1} \\
s^{(1)}_i &= s^{(0)}_i + \beta d^{(1)}_{i+1} + \beta d^{(1)}_{i} \\
d^{(1)}_i &= d^{(1)}_i + \gamma s^{(1)}_i + \gamma s^{(1)}_{i+1} \\
s^{(2)}_i &= s^{(1)}_i + \delta d^{(2)}_i + \delta d^{(2)}_{i+1} \\
\zeta &= \zeta s^{(2)}_i \\
d_i &= K \ast d^{(2)}_i \\
\end{align*}
\]

where \(x_{2i}\) is the even point and \(x_{2i+1}\) is the odd point of the input signal. \(s_i\) and \(d_i\) are the wavelet coefficients, \(\alpha, \beta, \gamma, \delta, \zeta\) are the wavelet lifting coefficients that are computed by liftwave(‘9.7’) function of matlab. The values of \(\alpha, \beta, \gamma, \delta, \zeta\) are as follow.

\[
\begin{align*}
\alpha &= \begin{bmatrix} -1.5861 & -1.5861 \end{bmatrix} \\
\beta &= \begin{bmatrix} 1.0796 & -0.0530 \end{bmatrix} \\
\gamma &= \begin{bmatrix} -0.8829 & -0.8829 \end{bmatrix} \\
\delta &= \begin{bmatrix} 0.4435 & 1.5761 \end{bmatrix} \\
\zeta &= -1.1496 \\
K &= 1/\zeta = -0.8699 \\
\end{align*}
\]

In our design, ECG signal is decomposed in a three layers structure with CDF9/7 wavelet above all. Then remove some high frequency coefficients of each layer with soft threshold. We use the processed coefficients to reconstruct ECG which will be used to detect R-waves.

Secondly, we use second-order differential to look for the maximum points of ECG. R-wave has high amplitude and greater slop in the ECG. So the maximum found in an RR interval can include the peak of R-wave. If \(x(n)\) is the original signal and \(N\) is the number of the signal, the used functions are

\[
x'_i(n) = \text{sign}(x(n) - x(n+1)) \begin{cases} 
1 & \text{rising part} \\
0 & \text{level part} \\
-1 & \text{dropping part} 
\end{cases} \quad n = 1, 2, \ldots, N-1.
\]

\[
x''_i(n) = \text{sign}(x'_i(n) - x'_i(n+1)) \begin{cases} 
2 & \text{minimum} \\
-2 & \text{maximum} \quad n = 1, 2, \ldots, N-2.
\end{cases}
\]

where \(x'_i(n)\) is the value of first difference, \(x''_i(n)\) is the value of second difference, sign is sign function. When \(x''_i(n) = -2\), record the data in the array named M. The records include location information and amplitude information.

At last, we computed the threshold based on integral projection function, which is according to the distribution characteristics of the maximum we found in ECG. The signal amplitudes of the maximum from M are divided into 16 parts evenly and the content of each part are recorded in the array named \(Th\). \(Th\) is computed from

\[
Th(i) = \min(M) + i \times \frac{\max(M) - \min(M)}{16} \quad 1 \leq i \leq 16, i \in Z
\]

Then design an integral projection function:

\[
S(i) = \sum_{j=i}^{i} I(x) \quad 1 \leq i \leq 16, i \in Z
\]

where

\[
y(i) = \min(M) + i \times \frac{\max(M) - \min(M)}{16} \quad 1 \leq i \leq 16, i \in Z
\]

\[
I(x) = \begin{cases} 
1 & \text{maximum} \\
0 & \text{others} 
\end{cases}
\]

Select i value of the intersection of zero distribution and non-zero distribution, then compute \(Th(i)\). The threshold of R-wave \(R_{th}\) equals \(Th(i)\). After computing the threshold \(R_{th}\), we record the maximum points whose value are larger than \(R_{th}\) and mark them as R-wave points.

In the following contents, we will elaborate that how to implement the algorithm on FPGA.

III. DESIGN AND IMPLEMENTATION ON FPGA

R-wave detection in our design is based on CDF9/7 wavelet filter and differential method. In this design, we use data from MIT-BIH arrhythmia database as our input data. The hardware design is based on Altera DE2-70 development board whose chip is Cyclone® II EP2C70F896C6, which includes FPGA
In the design, the FPGA chip is taken as the central microprocessor and is applied structured design on Verilog to realize ECG signal processing. The ECG data would be stored in SDRAM on FPGA board. After analyzed processed signal with PC, RS232 serial communication is chosen. State indicator light is used to indicate different steps of system operation.

Fig.3 shows the inner function diagram of the FPGA. As we can see in Fig.3, the whole designs are divided into four modules, which are CDF9/7 wavelet filter module, extreme point detection module, threshold setting and R-wave detection module and clock generator module. The FPGA designs of CDF9/7 wavelet filter module and extreme point detection module are very important parts in this design. Based on the hardware system, we take full account of the structure of CDF9/7 wavelet filter and extreme point detection algorithm in our design to reduce the cost of resources and improve the detection accuracy.

The functions and implementation details of each module will be described in the following sections.

A. FPGA Design of CDF9/7 Wavelet Filter

The ECG signal is decomposed in a three layers structure with CDF9/7 wavelet in the design, so the wavelet transform process consists of three steps. The data processing is single flow, namely, the out of low-frequency signal is the input of wavelet transform in each level of the wavelet decomposition, therefore the use of the pipeline design method that is one of the famous design ideas and skills in the FPGA design can greatly improve the working performance of the system. The block diagram of CDF9/7 wavelet transform module is shown in Fig.4.

As we can see, wavelet transform sub-module is a multiply or multiply accumulate operation. In Fig.5, the ECG data is stored in SDRAM. Wavelet lifting coefficients are saved as parameter variables. Each wavelet lifting coefficient is expanded 2^{16} times before it is saved. The transfer function is \( C = P \times 2^{16} \). \( P \) is wavelet lifting coefficients before processed. \( C \) is wavelet lifting coefficients after processed. Wavelet lifting coefficients saved is integer part of \( C \). Multiplier design is implemented by circuit \( \text{REG} = (C \times 2^{16} + 32768) >> 16 \). \( C \) is the wavelet lifting coefficients after processed. \( X \) is the ECG data. The results that are calculated by the multiplier have error compared with the IP core ALTFP_MULT, but according to the experimental results, the error does not affect the final detection results, so multiplier designed based on this method is in full compliance with the design requirements, and this multiplier can also be used in some designs which the requirements for results of calculation precision is not very high. In this design, this multiplier simplifies float operation to integer calculation and shift operation, which leads to reduce the cost of resource, improve the speed of operation, and it is very convenient for hardware implementation. Accumulator accumulates the results gained by the multiplier and output results through the register.

The decomposed signal is reconstructed after filtering. In the design, the implement of filters threshold is according to the method in [18].

B. FPGA Design of R-wave Detection

1) Extreme Point Detection: Extreme point detection is one of the most important parts of R-wave detection. Its accuracy directly affects the accuracy of the results of R-wave detection. Maximum points are used in this design. The diagram of extreme point detection is shown in Fig.6.
We set a memory variable Temp in the module of implementing first-difference. The variable Temp can store two 12-bit data. The ECG data is stored in the Temp at the rising edge of the clock and we calculate the first difference through the circuit \( \text{diff1} = \text{Temp}[1] - \text{Temp}[2] \). In the design of sign function module, we use the method of state machine and judging the sign bit of data. Data is stored in the form of complementation in the FPGA. Therefore, the sign bit can determine a number is positive or negative. The state diagram is shown in Fig.7.

![Fig.6 The diagram of extreme point detection](image)

**2) R-wave Detection:** The process of R-wave detection is similar to the process of maximum point detection, which choose the values greater than threshold value from the maximum stored in the RAM and record the correspond addresses. In the design, threshold is computed by state machine. We design sixteen states to calculate integral projection function and gain the threshold value for R-wave detection.

The algorithm flowchart which is used to implement R-wave detection is shown in Fig.8. After the overall analysis is completed, the information of R-wave is displayed.

**C. FPGA Design of Clock Generator Module**

Clock module generates working clocks for other modules. In this design, we use IP core ALTPLL. The input clock of ALTPPLL is 50MHz, which is provided by clock pin PIN_AD15 of FPGA chip. The output signals of ALTPPLL are clocks, which are provided for the other working modules. Therein, the clock of SDRAM has a negative phase shift of sixty five degrees.

**IV. VALIDATION AND RESULTS**

The well-known MIT/BIH arrhythmia database [19] is used to test accuracy of the system. We download the programs into the FPGA chip using USB cable and FPGA chip generates circuits that are integrated all the modules. The system of maximum clock frequency is 50MHz. The application status of resources is shown in Table 1. We can know that the utilization rate of resources is low, just 6%. In the design, a large number of resources are left. So it is possible that consummating this system and adding some other functions, such as wireless communication, LCD screen display, etc.
All experiments based on FPGA are completed with Quarti II 9.0 and the hardware system platform is Pentium(R) 4 CPU 515J @ 2.93GHz, 1G DDRII with Windows XP. In the design, we confirm the design and implementation of FPGA by using a SignalTap II Embedded Logic Analyzer (ELA), which designers can observe the behavior of hardware (such as peripheral registers, memory buses and other components) in response to software execution.

Table I. Device Utilization Summary

<table>
<thead>
<tr>
<th>Resource name</th>
<th>Occupied</th>
<th>Total</th>
<th>Proportion</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logic elements</td>
<td>3927</td>
<td>68416</td>
<td>6%</td>
</tr>
<tr>
<td>pins</td>
<td>40</td>
<td>622</td>
<td>6%</td>
</tr>
<tr>
<td>Memory bits</td>
<td>137668</td>
<td>1152000</td>
<td>12%</td>
</tr>
<tr>
<td>PLLs</td>
<td>1</td>
<td>4</td>
<td>25%</td>
</tr>
<tr>
<td>registers</td>
<td>958</td>
<td>-</td>
<td>--</td>
</tr>
</tbody>
</table>

In this paper, the presented implementation schemes of the R-wave detection algorithm based on FPGA chip have a latency of 6 clock cycle. This is because determining whether a sample value is R-wave, large sample values needs to be processed. In Ref. [15], A. Shukla designs the QRS detection system based on the FPGA. It takes four minutes and forty-three seconds to analyze thirty minutes ECG signal. Compared with the implementation method in the design, it has more delay. The testing results of ref. [15] are shown in Table II, which are comparable with the current design. According to the utilization rate of resources, A. Shukla’s implementation method used 75% resources, which is much more than current design in this work.

V. CONCLUSION

This paper describes an implementation method of real-time R-wave detection using FPGA. The algorithm is implemented with Altera Cyclone® II EP2C70F896C6. The prototype system has been tested in real-time. The results show that the system can detect R-wave accurately and is very good for ordinary R waves. In our design, we use pipeline design method and state machine, which are famous design ideas and skills in FPGA design, to improve the working efficiency of the system. The multiplier simplifies float operation to integer calculation and shift operation, which leads to reduce the cost of resource, improve the speed of operation. In the design, the utilization percent of resource is low, so more other modules can be easily join this design to form a larger system with more functions.

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