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A miniature high-efficiency fully digital adaptive voltage scaling buck converter

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A miniature high-efficiency fully digital adaptive voltage scaling (AVS) buck converter is proposed in this paper. The pulse skip modulation with flexible duty cycle (FD-PSM) is used in the AVS controller, which simplifies the circuit architecture (<170 gates) and greatly saves the die area and the power consumption. The converter is implemented in a 0.13-μm one-poly-eight-metal (1P8 M) complementary metal oxide semiconductor process and the active on-chip area of the controller is only 0.003 mm², which is much smaller. The measurement results show that when the operating frequency of the digital load scales dynamically from 25.6 MHz to 112.6 MHz, the supply voltage of which can be scaled adaptively from 0.84 V to 1.95 V. The controller dissipates only 17.2 μW, while the supply voltage of the load is 1 V and the operating frequency is 40 MHz.

Keywords: adaptive voltage; dynamic voltage; voltage scaling; low voltage; low power

1. Introduction

In a synchronous complementary metal oxide semiconductor (CMOS) digital circuit operating at a high speed, the main power consumption is caused by switching of logic gates, which can be expressed as 

\[ P = \alpha f_{\text{clk}} CV_{\text{dd}}^2 \]

where \( \alpha \), \( f_{\text{clk}} \), \( C \) and \( V_{\text{dd}} \) are the activity factor, the operating frequency, the total switching capacitance and the supply voltage, respectively (Burd, Pering, Stratakos, & Brodersen, 2000; Devlin, Ikeda, & Asada, 2011; Kang, Kim, & Doyle, 2006; Lee, Kim et al., 2012; Ma & Bondade, 2010; Wei & Horowitz, 1999). The supply voltage of digital load can decrease in accordance with decrease of working frequency without causing timing error. However, the period of time to complete a task increases with the reduced frequency, which is \( T = N \cdot (1/f_{\text{clk}}) \) where \( N \) is the number of clock cycles necessary to accomplish the given task (Ma & Bondade, 2010). As a result, the energy required to accomplish the given task is \( E = \alpha NCV_{\text{dd}}^2 \) (Abdallah & Shanbhag, 2010; Hanson et al., 2006; Kim & Agrawal, 2011; Ma & Bondade, 2010; Markovic, Wang, Alarcon, Liu, & Rabaey, 2010; Ramadass & Chandrakasan, 2008). So, it is a better method for energy saving to reduce the supply voltage properly at a given operating frequency.

There are two basic ways to reduce power consumption by lowering \( V_{\text{dd}} \): dynamic voltage scaling (DVS) and adaptive voltage scaling (AVS) (Barai, Sengupta, & Biswas, 2010; Burd et al., 2000; Das et al., 2009; Dhar & Mortensen, 2005; Drake et al., 2007;
Ikenaga et al., 2012; Kang et al., 2006; Lee, Chiu et al., 2012, Lee, Huang, et al., 2012; Nakai et al., 2005; Nowka et al., 2002; Wei & Horowitz, 1999; Zhen, Zhu, Luo, He, & Zhang, 2013). DVS is an open-loop approach that is based on the selection of operating points from a predefined $f_{clk}-V_{dd}$ look-up table. However, each operating point must be suitably margined to guarantee computational correctness in the worst-case combination of process, voltage and temperature (PVT) conditions. AVS is a closed-loop approach whose operating points are based on the operating frequencies.

In order to select an optimal supply voltage for a given operating frequency, various AVS techniques have been developed. In Razor (Das et al., 2009; Fojtik et al., 2013), an aggressive approach is developed for processor pipelines, where the voltage margin is eliminated and the system can dynamically detect and correct timing errors. The supply voltage is adjusted according to the detected error rate, allowing the system to operate with minimum supply voltage and maintain a small error rate. However, error handling needs auxiliary circuits and consumes time and energy. The critical path replica (CPR)-based approach eliminates a subset of the worst-case margin (Burd et al., 2000; Drake et al., 2007; Elgebaly & Sachdev, 2007; Ikenaga et al., 2012; Kang et al., 2006; Kuroda et al., 1998; Ma & Bondade, 2010; Nakai et al., 2005; Wei & Horowitz, 1999). The replica delay is monitored whose supply voltage and operating frequency are scaled until the replica just about fails to meet timing. The replica tracks the critical path delay of the digital load across different combinations of PVT.

A miniature high-efficiency fully digital AVS buck converter is proposed in this paper. In SoCs with multiple on-chip voltage and frequency domains with each domain having a specific power requirement, the proposed AVS controller can minimise the layout area, the power consumption and other associated penalties of the power delivery system. Section 2 describes the implementation of the proposed AVS buck converter. The experimental results are proposed in Section 3. Section 4 concludes the paper and summarises this work.

2. Implementation of the proposed AVS buck converter

2.1. System architecture

The block diagram of the proposed AVS buck converter is shown in Figure 1. The controller consists of a load delay monitor and a pulse skip modulation with flexible duty cycle (FD-PSM) control circuit. The load delay monitor includes a delay detector and a CPR whose delay reflects the delay of digital load. The load is a synchronous CMOS digital circuit. $V_{in}$ and $V_{out}$ are the input and output voltages of the converter, respectively. $V_{out}$ is fed back to the CPR. TR is the result of the delay monitor, according to which the FD-PSM control circuit generates control pulses with flexible duty cycle to turn on or turn off the power switch MP. As a result, the supply voltage of the load is regulated. CLK_REF is the operating clock of digital load. Once the frequency of CLK_REF is changed, by using feedback, the supply voltage of load will be scaled adaptively to guarantee its normal operation without timing error. CLKM is a clock with constant frequency and duty cycle.

2.2. Circuit implementation

Suppose $V_{ref}$ is the expected voltage of digital load,

$$TR = \begin{cases} 
0, & (V_{out} \geq V_{ref}) \\
1, & (V_{out} < V_{ref}) 
\end{cases}$$

(1)
TR = 1 represents that the output voltage is lower than $V_{\text{ref}}$ and TR = 0 represents that the output voltage is larger than or equal to $V_{\text{ref}}$. The FD-PSM control circuit will generate control pulses with different duty cycles to control the switching of MP, Power switch is
\[
\begin{cases} 
\text{turned on,} & \text{CLKM} = 1 \text{ and } TR = 1 \\
\text{turned off,} & \text{CLKM} = 0 \text{ or } (\text{CLKM} = 1 \text{ and } TR = 0)
\end{cases}
\]

The schematic of the proposed AVS controller is shown in Figure 2, which consists of a load delay monitor and an FD-PSM control circuit. The load delay monitor consists of a D flip-flop (DFF1), a T flip-flop (TFF2), a 2-input XOR gate (XOR1), a 2-input NOR gate (NOR1) and a CPR. The CPR is a delay line which consists of NOR gates. The CPR delay is $t_d$. CLKTD is obtained by delaying CLKT a CPR's delay. At each rising edge of CLK2, the comparison result of CLKT and CLKTD is latched by DFF1 and TR is updated. If CLKT = CLKTD at the rising edge of CLK2, OX which is logic low is latched by DFF1 and TR is updated, which shows that $V_{\text{out}}$ is high enough and the digital load can operate without timing error. If CLKT $\neq$ CLKTD at the rising edge of CLK2, OX which is logic high is latched by DFF1 and TR is updated, which shows that $V_{\text{out}}$ is not high enough to guarantee the normal operation of digital load and the output voltage of the converter should be increased. The timing diagram of the load delay monitor is shown in Figure 3a.

The CPR shown in Figure 2b consists of two parts, the delays of which are $\tau$ and $\Delta \tau$. The delay $\tau$ is the same as the delay of the critical path of load. $\Delta \tau$ is the delay margin which is added to guarantee the error-free operation of the load over various worst-case combinations of PVT.

FD-PSM technique is used to generate the control pulse of the power switch. Compared with the MDR modulation technique (Qin & Xu, 2010), FD-PSM technique is easier to realise and more duty cycles can be used to control. The FD-PSM control circuit is shown in Figure 2c. During CLKM = 0, both nodes B and GATE will be logic
If $TR = 0$ at the rising edge of $CLKM$, the power switch will be turned off and be kept off in the current switching cycle. If $TR = 1$ at the rising edge of $CLKM$, the power switch will be turned on. Afterwards, once $TR$ becomes from logic high to logic low in the current switching cycle, the power switch will be turned off immediately and be kept off in the remaining time of this switching cycle.

During $CLKM = 1$, if $TR$ keeps logic high, the power switch will be kept on for an entire duty cycle of $CLKM$. The timing diagram of the proposed AVS buck converter is shown in Figure 3.

During the operating process of the AVS buck converter over variations of PVT, there is a maximum nonzero duty cycle $D_{\text{max}}$ which equals the duty cycle of $CLKM$, a zero
Figure 3. The timing diagram of the proposed AVS buck converter: (a) Load delay monitor and (b) FD-PSM control circuit.
duty cycle $D_0$ (or skipping pulse) and a series of middle duty cycles. The middle duty cycle is denoted by $D_i^*$ and there is $0 < D_i^* < D_{\text{max}}$.

The maximum output voltage, the minimum output voltage, the maximum input voltage and the minimum input voltage of the AVS buck converter are $V_{\text{out,max}}$, $V_{\text{out,min}}$, $V_{\text{in,max}}$ and $V_{\text{in,min}}$, respectively. The clock cycle time of digital load is $T_{\text{clk}}$. $t_d \leq T_{\text{clk}}$ means that the output voltage of the buck converter is too high and skipping pulse will occur. $t_d > T_{\text{clk}}$ means that the output voltage of the buck converter is too low and the power switch will be turned on. But the on-time of the power switch will not be longer than $D_{\text{max}}T_{p}$. During the on-time, once $t_d$ reaches $T_{\text{clk}}$, the power switch will be turned off immediately and the duty cycle of this switching cycle is $D_i$ ($0 \leq D_i \leq D_{\text{max}}$). The maximum duty cycle which can be used in the proposed AVS buck converter operating in DCM is $D_{\text{max}} = \frac{V_{\text{out,min}}}{V_{\text{in,max}}}$.

### 2.3. Stability analysis

Based on the energy conversion principle, for the proposed AVS buck converter shown in Figure 1, the energy transferred from the power supply $V_{\text{in}}$ during a switching cycle can be expressed as

$$\Delta E_{\text{in}} = \Delta E_L + \Delta E_C + \Delta E_R$$

(3)

where $\Delta E_L$, $\Delta E_C$ and $\Delta E_R$ are the variation of energy stored in the inductor, the variation of energy stored in the filtering capacitor and the energy absorbed by the digital load during this switching cycle, respectively.

$\Delta E_{\text{in}}$ is the input energy from the power supply each switching cycle with duty cycle $D_i$. For the AVS buck converter operating in the steady state, the expected output voltage is denoted by $V_{\text{ref}}$, and the actual output voltage at the beginning of the switching cycle is denoted by $V_{\text{out}}$. In the presented buck converter, the peak current of the inductor can be expressed as $I_{pk} = (V_{\text{in}} - V_{\text{out}})D_iT_p/L$ and $\Delta E_{\text{in}}$ can be expressed as

$$\Delta E_{\text{in}} = V_{\text{in}} \int_{0}^{D_iT_p} i_L \, dt = V_{\text{in}} \cdot \left( \frac{1}{2} D_i T_p \cdot I_{pk} \right) = \frac{V_{\text{in}}(V_{\text{in}} - V_{\text{out}})T_p^2}{2L} D_i^2$$

(4)

where

$$D_i = \frac{-b + \sqrt{b^2 - 4ac}}{2a} \text{ and } \begin{cases} a = 0.5T_p^2V_{\text{out}}(V_{\text{in}} - V_{\text{out}})/L \\ b = -\tau T_p E_{C,nT_p} - 0.5\tau C_L V_{\text{ref}}^2 T_p \\ c = E_{C,nT_p} - 0.5 C_L V_{\text{ref}}^2 \\ \tau = 1/(R_L C_L) \end{cases}$$

(5)

$L$, $R_L$, $C_L$ and $i_L$ are values of the filtering inductor, the load resistor, the filtering capacitor and the inductor current of the buck converter, respectively. $E_{C,nT_p}$ is the energy stored in the filtering capacitor at the beginning of the $n$th switching cycle. To simplify analysis, the input voltage is assumed a constant. If $D_i > D_{\text{max}}$ in Equation (5), $D_i$ will be assigned $D_{\text{max}}$ forcibly. The maximum input energy is

$$\Delta E_{\text{in,max}} = \frac{V_{\text{in}}(V_{\text{in}} - V_{\text{out}})T_p^2}{2L} D_{\text{max}}^2$$

(6)
If $V_{\text{out}} \geq V_{\text{ref}}$ at the beginning of the switching cycle, skipping pulse will occur and $\Delta E_{\text{in}}$ can be expressed as $\Delta E_{\text{in}} = 0$.

Since the buck converter operates in DCM, $\Delta E_L = 0$. $\Delta E_C$ is the energy variation stored in the filtering capacitor from the beginning of the $n$th switching cycle to the beginning of the $(n+1)$th switching cycle, that is,

$$\Delta E_C = E_{C,(n+1)T_p} - E_{C,nT_p} = 0.5C_L(V_{C,(n+1)T_p}^2 - V_{C,nT_p}^2) \tag{7}$$

where $E_{C,(n+1)T_p}$ and $E_{C,nT_p}$ are the energy stored in the filtering capacitor at the beginning of the $(n+1)$th and the $n$th switching cycle, $V_{C,(n+1)T_p}$ and $V_{C,nT_p}$ are the voltage of the filtering capacitor at the beginning of the $(n+1)$th and the $n$th switching cycle. $\Delta E_R$ can be obtained as

$$\Delta E_R = \int_{nT_p}^{(n+1)T_p} [V_C(t)]^2/R_L]dt \approx T_P(E_{C,nT_p} + E_{C,(n+1)T_p})/(R_L C_L) \tag{8}$$

Substituting Equations (7) and (8) into Equation (3), $E_{C,(n+1)T_p}$ can be obtained as

$$E_{C,(n+1)T_p} = \frac{1 - T_P/(R_L C_L)}{1 + T_P/(R_L C_L)} \cdot E_{C,nT_p} + \frac{1}{1 + T_P/(R_L C_L)} \Delta E_{\text{in}} \tag{9}$$

For $T_P \ll R_L C_L$, there is $0 < [1 - T_P/(R_L C_L)]/[1 + T_P/(R_L C_L)] < 1$. The energy iterative model of the converter can be given, that is,

$$E_{C,(n+1)T_p} = \begin{cases} 
\lambda E_{C,nT_p} + \gamma \Delta E_{\text{in}} & (V_{\text{out}} < V_{\text{ref}}) \\
\lambda E_{C,nT_p} & (V_{\text{out}} \geq V_{\text{ref}}) 
\end{cases} \tag{10}$$

where $\lambda = (1 - T_P/(R_L C_L)) \cdot (1 + T_P/(R_L C_L))^{-1}$, $\gamma = (1 + T_P/(R_L C_L))^{-1}$.

Based on 999 times of iteration by using MATLAB, the simulation result of stability of the control loop is shown in Figure 4. The parameters for simulation are $V_{\text{in}} = 3.3$ V, $T_P = 0.6667$ $\mu$s, $C_L = 10$ $\mu$F, $L = 3.3$ $\mu$H and $D_{\text{max}} = 21.21\%$, which are also the circuit parameters for design and measurement of the test chip.

For the input energy that is proportional to the square of the duty cycle shown in Equation (4), the variation of the energy stored in the capacitor at the end of each switching cycle reflects the variation of the duty cycle. For the load shown in Figure 4a, the initial voltages of $V_{\text{out}}$ and $V_{\text{ref}}$ both are 1.2 V, and the load resistor is 50 $\Omega$. The energy stored in the filtering capacitor at the end of each switching cycle is lower than $0.5C_L V_{\text{ref}}^2$. Meantime, the output voltage of the buck converter at the end of each switching cycle is lower than $V_{\text{ref}}$, no skipping pulse occurs except in the initial switching cycle and all duty cycles keep close to $D_{\text{max}}$. With the decrease of load shown in Figure 4b, the maximum duty cycle $D_{\text{max}}$ still occurs, but the number of skipping pulses increases. In Figure 4c while the load is lighter, the maximum duty cycle which occurs is smaller than $D_{\text{max}}$ and more skipping pulses occur. Since the energy spreads in a small range in the simulation shown in Figure 4a–c, the control loop is always stable.
2.4. Ripple

Compared with the conventional PSM (Kapat, Patra, & Banerjee, 2011; Luo, Luo, Zhaoji, Yang, & Chen, 2002), more duty cycles can be used flexibly in FD-PSM and more conservative energy can be transferred to the load, which can achieve smaller output voltage ripples. The output voltage ripple of the conventional PSM-controlled buck converter in DCM is

$$\Delta V_{\text{out}} = \frac{1}{2LC_{L}} \frac{V_{\text{in}}}{V_{\text{out}}} D_{\text{P}}^{2} T_{\text{P}}^{2} (V_{\text{in}} - V_{\text{out}}) \left[ 1 - \frac{V_{\text{out}}L}{D_{\text{P}} T_{\text{P}} R_{L} (V_{\text{in}} - V_{\text{out}})} \right]^{2}$$  (11)

which is shown in Figure 5. In the conventional PSM, there is only one nonzero duty cycle $D_{\text{max}}$. In FD-PSM, there can be a series of middle duty cycles not larger than $D_{\text{max}}$. The colours red, blue and pink represent the simulation results when load resistors are 200 Ω, 100 Ω and 50 Ω, respectively (to view Figure 5 in colour, please see the online version of this journal). The symbols asterisk, solid line, plus sign, dot and dotted line represent simulation results when output voltages are 0.7 V, 0.9 V, 1.1 V, 1.3 V and 1.5 V, respectively.

In the FD-PSM-controlled buck converter, the maximum duty cycle which may occur decreases with the decrease of load current shown in Figure 4. It is shown in Figure 5 that the output voltage ripple also decreases with the decrease of the maximum duty cycle. The ripple of the FD-PSM-controlled buck converter is not larger than that of the conventional
PSM-controlled buck converter with the same $D_{\text{max}}$. Only when $D_i = D_{\text{max}}$, the ripple of the FD-PSM-controlled buck converter is equal to that of the conventional PSM-controlled buck converter.

### 3. Experimental results

The proposed AVS buck converter was fabricated in a 0.13-μm CMOS process. The chip micrograph of the AVS controller is shown in Figure 6. The area of the controller is only 0.003 mm$^2$ which is much smaller. The controller dissipates only 17.2 μW, while the supply voltage and the operating frequency of load are 1 V and 40 MHz, respectively. According to

$$E_s = \frac{aNCV_i^2 - aNCV_i^2}{aNCV_i^2}$$  \hspace{1cm} (12)
where $E_s$, $V_i$ and $V_f$ are the percentage of energy saving, the initial voltage and the expected voltage of scaling, a maximum of 81% energy can be saved when the supply voltage of load is scaled from 1.95 V to 0.84 V.

The measured voltage scaling process of the AVS buck converter is shown in Figure 7. In the measurement, the load resistor is 100 Ω. The output voltage of the proposed AVS

![Figure 7](image-url)
buck converter can be scaled in the range from 0.84 V to 1.95 V to the varied operating frequency of load in the range from 25.6 MHz to 112.6 MHz. The clock frequency of load is scaled from 25.6 MHz to 64.4 MHz and then is scaled from 64.4 MHz to 112.6 MHz; the output voltage is scaled adaptively from 0.84 V to 1.17 V and then is scaled adaptively from 1.17 V to 1.95 V (Figure 7a). The clock frequency of load is scaled from 112.6 MHz to 79.1 MHz and then is scaled from 79.1 MHz to 36.2 MHz; the output voltage is scaled adaptively from 1.95 V to 1.34 V and then is scaled adaptively from 1.34 V to 0.9 V (Figure 7b). It is also shown that the proposed AVS buck converter is stable during the operating process.

The measured waveforms of CLKM, TR, GATE and LX are shown in Figure 8. When the load is heavy (Figure 8a), there is no skipping pulse and the maximum duty cycle $D_{\text{max}}$ occurs. When the load is light (Figure 8b), no skipping pulse occurs and the maximum duty cycle that occurs is smaller than $D_{\text{max}}$. When the load is light shown in Figure 8c, skipping pulses occur.

The measured transient response is shown in Figure 9. It is shown in Figure 9a that when the frequency of CLK_REF is scaled from 79.1 MHz to 112.6 MHz, the output voltage of the AVS buck converter is scaled adaptively from 1.34 V to 1.95 V in 280 $\mu$s. When the frequency of CLK_REF is scaled from 112.6 MHz to 79.1 MHz shown in Figure 9b, the output voltage of the AVS buck converter is scaled adaptively from 1.95 V to 1.34 V in 580 $\mu$s.

Figure 8. The measured waveforms of the input clock CLKM, the output of the load delay monitor TR, the control pulse GATE and the voltage of node LX under different load conditions: (a) $V_{\text{out}} = 1.95$ V, $f_{\text{clk}} = 112.6$ MHz; (b) $V_{\text{out}} = 0.9$ V, $f_{\text{clk}} = 36.2$ MHz; (c) $V_{\text{out}} = 0.84$ V, $f_{\text{clk}} = 25.6$ MHz.
Table 1 compares the adaptive DC–DC converters in (Burd et al., 2000; Kang et al., 2006; Lee, Chiu et al., 2012; Wei & Horowitz, 1999) with the proposed one, which shows that the proposed AVS controller has smaller active on-chip area, lower power consumption, larger operating frequency range and larger voltage scaling range.

Figure 9. The measured transient response of the output voltage when the clock frequency of CLK_REF is scaled. ST is the trigger signal of the clock frequency change.
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4. Conclusions

A miniature high-efficiency fully digital AVS buck converter is proposed in this paper. FD-PSM is used in the AVS controller, which simplifies the circuit architecture and greatly saves the die area and the power consumption. The converter is implemented in a 0.13-μm 1P8 M CMOS process, and the active on-chip area of the controller is much smaller. The measurement results show that the operating frequency and the supply voltage of the load can be scaled in a large range, while the power consumption of the controller is much lower. The proposed AVS buck converter is very suitable for multiple voltage and frequency domain applications with each domain having a specific power requirement.

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