A Continuously and Widely Tunable 5 dB-NF 89.5 dBi-Gain 85.5 dB-DR CMOS TV Receiver With Digitally-Assisted Calibration for Multi-Standard DBS Applications

Song-Ting Li, Jian-Cheng Li, Xiao-Chen Gu, Hong-Yi Wang, Ming-Hua Tang, and Zhao-Wen Zhuang

Abstract—This paper presents a direct-conversion, multi-standard TV receiver implemented in a 0.13 μm CMOS technology occupying less than 4 mm². The receiver is compliant with several direct broadcasting satellite (DBS) standards, including DVB-S, DVB-S2, and ABS-S. A novel automatic frequency tuning (AFT) technique is adopted based on a searching algorithm to ensure less than 6% bandwidth deviation of the different bandwidths (over 40 bandwidth channels) for multi-standard applications. Moreover, digitally-assisted DC offset calibration is used to improve second-order distortion and calibration time of the receiver and the residual output offset achieved is less than 3 mV. An integrated ΣΔ fractional-N synthesizer utilizing an optimized automatic frequency calibration (AFC) scheme enables a fast and high-precision calibration process for dual-VCO phase-locked loop (PLL) operation. The measured linearity exceeds the desired target with the minimum margin in excess of 7 dBm, and the maximum carrier-to-noise ratio (CNR) values are better than 30 dB over wide input power levels, ensuring robust reception in variable environments. All circuit blocks are operated at 2.8 V stabilized by an LDO and consuming a total current of about 56 mA.

Index Terms—ABS-S, automatic frequency tuning (AFT), DC offset calibration (DCOC), direct-conversion receiver, DVB-S, DVB-S2, widely-tunable high-precision filter, automatic frequency calibration (AFC).

I. INTRODUCTION

Despite the increasing progress observed in wireless terrestrial communication networks, satellite systems remain an appealing solution for broadcasting, point-to-point, and multicasting telecommunications, because of undemanding customer equipment and wide coverage capability. In this scenario, the DBS service is being deployed in most countries to provide multimedia business like digital TV using a variety of standards. To allow for user flexibility and enable economies of scale for terminal manufacturers, digital TV receivers supporting multiple DBS standards are desired. In satellite broadcast TV, the most dominant standards expected to co-exist are digital video broadcasting-satellite (DVB-S) from Europe based on QPSK modulation, its improved version DVB-S2 and Chinese advanced broadcasting system-satellite (ABS-S), both based on QPSK or 8PSK modulation. All of them are developed using the Ku-band (10.7–12.75 GHz) or C-band (3.4–4.7 GHz) for air-transmission and using the L-band (0.95–2.15 GHz) for set-top box applications [1].

This paper presents a monolithic direct-conversion TV receiver containing DVB-S/S2 and ABS-S for DBS L-band applications. The multi-standard receiver supports wide RF band, arbitrary channel spacing and baseband bandwidths from 4.5 to 32 MHz.

Most broadcast-based digital TV RF receivers, published in the past have focused on the use of DVB-T/H standards [2]–[7], which also can handle the L-band signals, but these receivers lack sufficient bandwidth (typically below 8 MHz) to process the DBS signals. Several DBS L-band receivers [8]–[11] have been reported to process DVB-S/S2 standards with wide bandwidth range (over 40 different bandwidth channels ranging from 9 MHz to 60 MHz), however, the traditional AFT scheme [4],[12] adopted in these receivers compensates for the bandwidth deviation through tuning a capacitive or resistive array in the filter of the DBS receiver. It will consume more silicon area for the desired wide bandwidth range because the tuning mechanism requires a free degree of freedom (R or C) which is used to tune the bandwidth of the filter. The corresponding capacitors or resistors must be added if additional bandwidths shall be made available. Hence, in order to reduce chip area and cost, the automatic frequency tuning (AFT) circuit for bandwidth calibration presented in this paper searches for an appropriate cut-off frequency point within the designed bandwidths rather than acquires the desired bandwidth through adjusting capacitive or resistive arrays. Therefore, this mechanism has two free degrees of freedom to calibrate the bandwidth, which will significantly decrease the chip area for wide bandwidth range applications.

All the receivers mentioned above utilize a direct-conversion structure. In order to keep the DC offset related second-
order nonlinearity sufficiently low, the negative feedback servo loop based on an integrator topology is used [4], [12]–[14] in these receivers. However, this calibration scheme needs several feedback loops which will consume power and chip area. In this paper, the critical second-order distortion issue in the receiver is tackled by using a digitally-assisted DC offset calibration (DCOC) [15]–[17]. In addition to having no use for low cut-off frequency of the feedback loop to ensure that sub-carriers around DC are not affected too much, this digital technique also provides the benefits of circuits and substrate noise immunity, low power consumption, and fast settling time.

Furthermore, all sensitivity, blocking and intermodulation specifications of the different standards must be met. Implemented in a 0.13 μm CMOS process, this work focuses on the receiver design to tackle the challenges of the trade-offs among noise, linearity, power consumption, silicon area and external bill-of-materials (BOM). Sections II and III discuss the system design challenges in detail and consider the architecture of the RF receiver, respectively. Section IV describes circuit implementation in detail. Section V reports the experimental results, and Section VI concludes the paper.

II. MULTI-STANDARD RECEIVER DESIGN CHALLENGES AND REQUIREMENTS

Fig. 1 depicts the block diagram of a DVB-S/S2 & ABS-S system. The defined requirements are referred to the RF reference point. The entire receiver must meet the required sensitivity and CNR of −80 dBm and 9 dB for the 8PSK 7/8 modulation, respectively, under the data rate of 45 MS/s which leads to the most strict noise figure (NF) requirement. The required sensitivity translates into a required receiver NF of 7.2 dB. Assuming that the RF front-end NF has a nominal value of 3 dB and that its maximum voltage gain is 34 dB, the required NF of the analog baseband is less than 35 dB.

For the minimum data rate of 4.42 MS/s with QPSK 1/2 modulation, the sensitivity level of the DBS system should be −90 dBm or below. In order to deliver a signal with an amplitude of 400 mV peak-to-peak to the input of the ADC, a maximum gain of at least 86 dB of the receiver is required. The maximum received signal strength is −5 dBm for 8PSK 7/8 modulation and about −15 dBm for QPSK 1/2 modulation. Hence, the required dynamic range (DR) of the RF receiver is 75 dB. 36 dB of the required DR is contributed by RF front-end, the remainder is taken into account for the analog baseband. To meet the requirement of the DR and to alleviate the complexity of the programmable gain amplifier (PGA), the low-pass filter (LPF) in the receiver provides an 18 dB gain range from −6 to +12 dB with steps of 6 dB. The residual 31.5 dB is provided by PGA with steps of 0.5 dB with a DR margin of about 10 dB. Assuming the entire DR of the receiver extends from 4 dB to 89.5 dB, the DR of the PGA should range from 12 dB to 43.5 dB under condition that maximum gain and DR of the RF front-end are 34 dB and 36 dB, respectively.

DBS service is characterized by the fairly large frequency band to be received (extending 1 GHz), and referred to as wideband system. In contrast to narrow-band system such as cellular and cordless communications, DBS receivers suffer from a large number of unwanted channel interferers because of the many broadcasting channels and satellites. Moreover, for the C-band DBS service, the out-of-narrowband signals (e.g., from wireless local area network (WLAN)) also generate serious second-order inter-modulation distortion (IMD2) and third-order inter-modulation distortion (IMD3), respectively. Therefore, stringent linearity requirement must be achieved in the DBS receiver.

As shown in Fig. 2, worst case conditions for the linearity requirement of an RF receiver are given in the case that strong out-of-band interferers such as WLAN in the 5 GHz band as well as adjacent-band interferers cause serious carrier-to-noise ratio (CNR) degradation. The test case defines two interferers allocated at 5.2 GHz and 5.7 GHz (WLAN 802.11a) with a power level of −4 dBm for the DVB-S/S2 C-band mode. If the pre-filter of the antenna in front of the receiver provides 36 dB attenuation for these interferers, the IIP3 of the receiver is −12.5 dBm under condition that the required sensitivity and CNR are −80 dBm and 9 dB, respectively. The required IIP3 introduced by the adjacent-band interferers exceed the input signal power of about 5 dBm, which can be ignored when the input power is very small. It is obvious that the most crucial condition to the baseband chain IIP3 is given by WLAN 802.11a interferers because they will also generate IMD3 in the desired band after down-mixing. Therefore, the required out-of-band IIP3 of the baseband chain shall be more than 14 dBm at the maximum RF front-end gain setting of 34 dB. The interferers also may cause IMD2 for DVB-S/S2 before down-mixing. To avoid CNR degradation, the input-referred second-order intercept point (IIP2) must exceed 10 dBm for the RF receiver, and the IIP2 of the baseband chain should exceed 38 dBm at the maximum RF front-end gain setting of 34 dB when WLAN 802.11a interferers exist.

In order to ease the linearity requirement of the PGA at the last stage of the receiver, the LPF should attenuate the adjacent-band and out-of-band interferers as strong as possible. Otherwise, the PGA will at least require an IIP3 of 30 dBm and an IIP2 of 53.5 dBm, respectively, which is difficult to maintain the linearity during adjusting the gain of the PGA. A compromise between complexity and performance is taken, a fifth-order Chebyshev LPF is adopted to provide about 20 dB attenuation at the frequency equals twice the cut-off frequency. Here, the required linearity for the PGA due to the out-of-band interferers can be ignored, and an IIP3 of 0 dBm and an IIP2 of 5 dBm are needed concerning the adjacent-band interferers, respectively.

For the sake of meeting different data rates from 4.42 MS/s to 45 Ms/s, the LPF cut-off frequency should be adapted in a wide range from 4.5 MHz to 32 MHz. Taking the scheme of the frequency tuning adopted in the LPF into account, 0.5 MHz...
steps from 3.5 MHz to 14 MHz and 1 MHz steps from 15 MHz to 40 MHz are implemented to satisfy the criterion that less than 6% cut-off frequency deviation is achieved.

According to the calculated specifications, Table I summarizes the multi-standard receiver requirements to satisfy the DVB-S/S2 and ABS-S applications.

### III. RECEIVER ARCHITECTURE

The receiver adopts the direct-conversion architecture to fulfill small physical size and low power consumption. A detailed block diagram of the receive implementation is presented in Fig. 3. The RF front-end including LNA, passive mixer and transimpedance amplifier (TIA) provide a maximum gain of 34 dB to suppress the noise contribution of the baseband. The single-ended-input differential-output LNA, or balun LNA [18], [19], facilitates the connection to the front antenna and to the following mixer using a double balanced topology. It eliminates the need of an off-chip balun in front of the LNA for low NF and low external bill-of-materials (BOM). Also, it does not require operation of on-chip balun after the LNA, as low distortion and low power consumption are achieved by this approach. Then, the DBS signals are down-converted to the baseband by the quadrature passive mixer. The TIA provides further attenuation of out-of-band interferers to ease the required linearity of the baseband chain. Moreover, it converts the current signals into the voltage domain. Subsequently, the analog baseband circuit removes the out-of-band interferers and amplifies the signal to the desired amplitude. Finally, the receiver produces I/Q balanced outputs for further signal processing at the baseband demodulator.

In this design, digitally-assisted automatic gain control (AGC) is included in both the RF front-end and the analog baseband to achieve the optimum CNR. In order to realize a large dynamic range with fine adjustment steps, the gain-distribution is arranged by distributing different gain ranges and steps among the stages, as listed in Table I. Furthermore, a digitally-assisted DCOC loop is adopted to eliminate the DC offset of the baseband chain to improve the IIP2 with fast calibration time and small residual output offset. An AFT circuit is integrated to ensure that the channel bandwidth only shows a weak process and temperature dependence. On this basis, the widely-tunable performance and high bandwidth precision are guaranteed simultaneously with less chip area than consumed in conventional implementation.

A ΣΔ fractional-N synthesizer is used for generation of the local oscillator (LO) signals (Fig. 3). This allows a wide range in selecting the external crystal reference, which ultimately can be shared with other applications to save cost, while maintaining a fine frequency step which is necessary for multi-standard operation. A high reference frequency and low output frequency of the voltage-controlled oscillator (VCO) make the phase-locked loop (PLL) division ratio N small and allow for using a high loop bandwidth, which reduces the overall integrated phase noise (PN) and outspread of the reference spur band. However, operation at higher VCO frequency enables the use of on-chip inductor with smaller area and higher Q factor. To maximize the obtained PN performance, the PLL covers a range from 1.8 to 4.5 GHz via two LC-VCOs. Quadrature LO signals for the L-band mixers are generated by division of the VCO frequency by 2.

All transistors in this receiver are 3.3 V thick-gate-oxide transistors from the given 0.13 μm CMOS process in order to provide better linearity and sufficient voltage headroom. All circuit blocks are operated at 2.8 V transferred from the I/O voltage of 3.3 V and buffered by internal LDOs to significantly improve the power supply rejection.

### IV. CIRCUITS IMPLEMENTATION

#### A. RF Front-End

Recently, a balun LNA concept has been successfully demonstrated by using the hybrid common-gate-common-source (CG-CS) amplifier topology, which does not only exhibit broadband single-to-differential conversion but also noise cancellation [4], [20], [21]. However, the NF of the conventional CG-CS topology is still poor, typically exceeding 3 dB. One method to resolve this issue is to increase the input transconductance of the CS amplifier and to decrease the load resistance accordingly to keep a balanced output at the expense of huge power consumption [22], [23].
As in [4], the proposed LNA shown in Fig. 4 utilizes the technique of dual cross-coupling to improve noise performance, and the source-degenerated inductor is replaced by transistors \( M_5, M_6 \) to save the chip area compared to the approach used in [4]. The capacitor \( C \) is inserted to provide the AC ground at the source stage of the \( M_9 \). The bulk cross-coupling incorporates an extra bulk-driven transconductor together with the conventional gate-driven one. The input transconductance is thus enhanced by 20% in such dual-gate transistor implementations without consuming extra DC current, which increases the voltage gain and reduces the noise contribution from subsequent stages. The cross-coupling capacitors \( (C_{c}) \) are used to reduce the contribution from M2 channel noise to 17.5% compared with the conventional level of 26% without increasing \( g_{m2} \) [4].

A pair of switch transistors \( M_{9,10} \) is inserted between conversion stage and current buffer \( (M_7-10) \) to provide a signal path for gain attenuation. When the switch transistors are turned off, the LNA is configured as cascaded two-stage amplifier, pro-
providing a transconductance of $g_{m1} R_{L,1}$, $g_{m7}$ with respect to input voltage. When the switch transistors are turned on and transistors $M_{8-10}$ are all off, the front-end is configured as one single-stage amplifier, providing a transconductance of $g_{m1}$ only. As a result, one-step gain attenuation of $g_{m7} R_{L,1}$ is achieved. This current-mode scheme effectively reduces the distortions introduced by voltage modulation in the conventional LNA design. Furthermore, the single-stage configuration has a higher current drive capability because of operating the CS amplifier with current source loads instead of resistors as in [4]. Moreover, in order to ensure impedance matching at both high gain mode and low gain mode, the scale of the transistors $M_7$ and $M_8$ must be designed carefully to ensure that the current through $M_1$ is constant at the two gain modes. The simulated results show that this switched path offers a stepped attenuation of 18 dB with a high IIP3 level of 2.5 dBm and an IIP2 level of 40 dBm, which are improved by about 10 dB and 12.5 dB, respectively, compared with the maximum gain configuration, while NF degrades by 5.5 dB only in the overall receiver chain.

Instead of using a Gilbert mixer, a current-mode down-converter is utilized to achieve high linearity and low flicker noise. The down-converter consists of two sets of passive CMOS mixers as shown in Fig. 4. Comparing this approach with traditional NMOS or PMOS passive mixers [24], the proposed CMOS topology obviously improves the even-order linearity of the down-converter by decreasing the DC leakage term introduced by the RF signal modulation effect [24]. Moreover, the gate and source DC voltage of the passive mixer must be carefully designed to ensure that the gate-source voltage $V_{GS}$ does not exceed the threshold voltage $V_T$ (i.e., $V_{GS} < V_T$), which guarantee that the $I-V$ curve of the passive mixer is stepwise to avoid occurrence of IMD2 due to the self-mixing of the RF input or the LO signal. Assuming the overdrive voltage $V_{GS} - V_T = V_I > 0$, the switch pair is operated in the on-state simultaneously at periodic time-slices (Fig. 5), which will introduce additional IMD2 components generated through the leakage of self-mixing DC components to exacerbate the IIP2 [25]. After down-conversion through the mixing quad, the baseband current is driven into the TIA based on an opamp-RC structure and then converted into voltage. The TIA is able to provide 18 dB dynamic range with 6 dB steps by adjusting the resistor $R_g$. The RF front-end achieves a maximum gain of 34 dB and minimum gain of $-2$ dB, and one tracked pole placed in the TIA can pre-filter the adjacent and out-of-band interferers to alleviate the linearity requirement of the baseband chain.

B. Analog Baseband

The analog baseband functions are channel selection and programmable amplification for both in-phase and quadrature signal processing. In this design, the analog baseband provides a total gain control from 6 to 55.5 dB with steps of 0.5 dB. Key circuit blocks are a widely-tunable variable-gain LPF, a wide dynamic range PGA, an AFT circuit, and a digitally-assisted DCOC loop.

We use a fifth-order active-RC Chebyshev LPF with 0.1 dB in-band ripple utilizing programmable capacitor and resistor arrays, as it provides better out-of-band interference attenuation, and better noise and linearity performance compared with Gm-C or Butterworth filters. The active-RC filter utilizes a RLC ladder structure to accomplish the fifth-order leapfrog rather than a cascade structure to acquire higher linearity. This structure, called the “main filter” is shown in Fig. 6. In order to achieve versatility of the multi-standard TV tuner, the cut-off frequency and pass-band gain are desirably controllable with the programming codes. In this design, the proper resistor and capacitor values are divided within the array configuration. Each element of the array can be accessed by external control signals to change the corresponding R and C values.

As the filter bandwidth covers the range of 3.5–40 MHz, the frequency band can be divided into 3.5–6.5 MHz, 7–13.5 MHz and 14–40 MHz. The first two bandwidth steps are 0.5 MHz, the latter ones 1 MHz. The high-frequency bandwidth range of 14–40 MHz with steps of 1 MHz is implemented by assigning different values to the capacitors of the capacitor array. In order to save further chip area, the required capacitance for generating new bandwidths frequency is created by adding or subtracting small capacitance values based on the original capacitance. Moreover, the first two low-frequency bandwidth ranges can be achieved via the multiplication of the resistance at fixing corresponding capacitance. Table II gives the distribution of bandwidths as a function of resistance and capacitance. It indicates that the coarse tuning (range selection) can be achieved through selecting the proper resistance, while the fine tuning (change with 0.5/1 MHz steps) through changing the capacitance.

Fig. 7 shows the architecture of the AFT loop in our design. The RC arrays are identical to those used in the main filter (Fig. 6). The accurate reference clock signals (CLK and inverted signal CLKn), which are generated by division of the VCO frequency by N.F to obtain the desired bandwidth, are used to con-
TABLE II
CUTOFF FREQUENCY OF LPF DISTRIBUTION

<table>
<thead>
<tr>
<th>Resistance ($R_c$)</th>
<th>Capacitance</th>
<th>Bandwidth</th>
<th>Step</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_c/2$</td>
<td>$C_{d}&amp;(C_1+C_2)$</td>
<td>14-40 MHz</td>
<td>1 MHz</td>
</tr>
<tr>
<td>$R_c$</td>
<td>the same as 14-27 MHz</td>
<td>7-13.5 MHz</td>
<td>0.5 MHz</td>
</tr>
<tr>
<td>$2R_c$</td>
<td>the same as 14-26 MHz</td>
<td>3.5-6.5 MHz</td>
<td>0.5 MHz</td>
</tr>
</tbody>
</table>

Fig. 6. LPF architecture.

Fig. 7. AFT circuit.

trol the MOS switches to decide the charging time of the capacitance array. The output voltage $V_{out,lpf}$ is compared with a reference voltage $V_{ref} (V_{dd}/2)$ corresponding to the desired $1/R_C$ time constant. The bandwidth selection module (BWS) (Fig. 8) adjusts the $RC$ arrays to an appropriate setting according to the comparator output result by the successive approximation (SAR) search. In this control loop, the output voltage can be expressed as

$$V_{out,lpf} = V_{dd}/(1 + f_{CLK} R_c C_c) \quad (1)$$

The BWS is integrated to avoid the appearance of a less optimum frequency code, which can be understood by considering the following example in Fig. 9. Here, we assume that the main filter only has a 3-bit frequency control code (FCC) for the sake of simplicity. The SAR algorithm will stop to work when the FCC of 011 is chosen. Nevertheless, from Fig. 9 it is not difficult to find that a FCC of 100 actually has the minimum bandwidth deviation. So we will calibrate the FCC with the help of BWS. During the bandwidth calibration process, the differential output of the oscillator (Fig. 10), whose frequency is $1/R_c C_c$ [26], is counted to $N_{clk}$ through the multi-phase counter (MPC) [27], [28] during a period $T_{GATE}$ which equals the high level duration of the clock signal CLK1 divided by $4 \times m$. There, $m$ is a variable which can be adjusted by the baseband chip. The target number $N_{clk}$ is obtained from the register which is written to 4$m$ in advance. Afterwards, the frequency error $\delta$ between the target frequency and the calibration frequency is generated by a comparator. A minimum error register in the bandwidth adjustment module (BA) is used to store the last minimum frequency error and its corresponding FCC. The FCCs involved in comparison only consist of the one provided by the SAR when the SAR process is finished and the adjacent FCCs, FCC + 1 or FCC − 1, respectively. The positive or negative sign can be determined by the result sign of the comparator. At last, the FCC corresponding to minimum frequency error will be chosen to calibrate the bandwidth of the main filter through the encoder. The high bandwidth frequency will be chosen if the minimum errors are the same to guarantee the integrality of the desired signal. At high frequencies within the given bandwidth, the frequency precision even can lower to less than 3% with the help of BWS.

Fig. 11 shows simulation results of the AFT calibration process in the time domain and the main filter frequency response when the resistors scale down by 10% for 10 MHz bandwidth. The AFT circuit can lock the desired cut-off frequency with seven steps via the SAR algorithm and BWS and achieves less than 6% frequency deviation.

The PGA is a key module in the receiver to obtain sufficiently high DR, so that it should provide a gain range as wide as possible and a step precision as small as possible to guarantee stability of the output signal. As shown in Fig. 12, the PGA adopts the current-mode-based gain adjustment rather than feedback-resistor-based not to exacerbate the channel selectivity of the entire receiver. In order to avoid the noise performance deterioration due to the common-gate NMOS-transistor pair while adjusting the variable source-degenerated resistance to change the gain of the PGA, the fully differential capacitor-cross-coupled topology from [29] is a good candidate thanks to its low NF and wide dynamic range. The variable source-degenerated resistor is composed of
eight NMOS-transistors which are controlled by 3-bit coarse tuning encoder and 6-bit fine tuning digital-to-analog converter (DAC). The NMOS-transistors work in the triode region with an equivalent resistance proportioned to gate-source voltage. The coarse tuning encoder serves as master controlling the ON/OFF state of each transistor to achieve coarse steps of 4.5 dB, and the fine tuning DAC controls the gate voltage of the corresponding transistor in ON-state to enable fine steps of 0.5 dB. The overall gain range of the PGA extends from 12 dB to 43.5 dB.

DCOC is indispensable in a direct-conversion receiver because DC offsets may saturate the baseband output and degrade second-order linearity. The basic approach of a digitally-assisted DCOC is to detect the DC offset component at the balanced output, then convert it into a corresponding digital signal, and generate a voltage or current step to be subtracted from the input or to be added to the input to adjust the output offset.

The DCOC circuit in this paper extends over the entire chain starting from the TIA and ending at the last PGA. Initially, DCOC is performed as the receiver is powered-on and before it receives the first symbol of data. The calibration process is.
successive to assure that the every module works correctly. Due to the fact that DC offset varies with temperature, DCOC needs to be re-executed every time slot when switching the operation state. The residual output offset after DCOC is designed to yield less than 3 mV by selecting the design parameter properly.

The digitally-assisted DCOC adopted here is implemented by a 1-bit quantizer and several 8-bit DACs combined with SAR algorithm digital control logic (Fig. 3). Considering the DCOC for the LPF, as shown in Fig. 12, for example, the DAC steals current from the LPF or releases current to it through evaluating the sign of the output to eliminate DC offset of its balanced branches. The DAC is composed of 256 resistors in series and it has two output voltages $V_3$ and $V_4$ which change contrarily with the alternation of the 8-bit digital input. The DCOC range and precision are dependent on output range and LSB step voltage of the DAC, respectively. In this design, the full range of the DAC is larger than 0.5 V while the LSB is less than 2 mV. We obtain less than 3 mV residual output offset by selecting appropriate resistance values for $R_{12}$. For other blocks, we also obtain less than 3 mV residual output offset by the same technique. Our DCOC circuit uses an auto-zeroing comparator [9] to compensate for the offset of the comparator itself. Simulation results of the DCOC circuit in the time domain are presented in Fig. 14. The calibration time of about 4 $\mu$s is very fast compared to the calibration time of 5 ms in [12] and 100 $\mu$s in [14] based on negative feedback.

C. Frequency Synthesizer

A fractional-N PLL synthesizer (Fig. 3), is employed to generate a wide frequency output from 1.8 to 4.5 GHz by using two LC-VCOs with overlapping tuning characteristics. The 22-bit fractional part of the division ratio is modulated by a third-order MASH $\Sigma$–$\Delta$ modulator achieving a frequency resolution of less than 50 Hz. In order to provide 4-phase LO signals for the quadrature mixer, the VCO works at twice the LO frequency and its output frequency is then divided by 2. As far as phase noise is concerned, the tuning range of each VCO is divided into 32 sub-bands by a 5-bit capacitor bank to decrease the voltage-to-frequency gain.

The proposed optimized AFC, which is similar to the BWS circuit, is composed of a frequency detector (FD) and a finite state machine (FSM) to select an optimal VCO tuning. A detailed block diagram of the proposed AFC is depicted in Fig. 15. The VCO output, whose frequency is equal to $f_{VCO}$, is first divided by 4 to lower the input frequency of the AFC. Then, $f_{DIV}$ is counted to $N_{car}$ during a period $T_{GATE}$. The target value $N_{dec}$ is obtained by multiplying the division ratio N.F with the parameter $m$. Here, $m = 2^4$ is chosen in this design which indicates $N_{dec}$ includes the integer part and 4 MSBs of the fractional part of the desired division ratio N.F. The overall calibration process of the proposed AFC technique can be divided into two steps, which are step 1 “minimum error search” and step 2 “optimal code selection”. In the first step, the low-band VCO and the high-band VCO are calibrated successively, and the minimum frequency error code for each VCO is stored in the register. In step 2, the minimum frequency error of low- and high-band VCO are compared, the low-band frequency code $FC_{LH}$ is fed to low-band VCO and the low-band VCO is enabled if the minimum errors are
the same since the low-band VCO will dissipate less power in this case, otherwise the one with smaller error will be chosen. Moreover, a multi-phase counter (MPC) [27], [28] is proposed instead of a conventional counter [30] to achieve that the calibration accuracy is not deteriorated even though the counting process is twice as fast as before. The total lock time, including coarse tuning and fine tuning, is less than 50 μs when the reference clock is 27 MHz.

The loop filter is of third order to suppress the out-of-band phase noise generated by the $\Sigma – \Delta$ modulator. The loop filter is
implemented with the resistance and capacitance arrays to support the multiple reference clocks. The source and sink currents of the charge pump are varied from 40 to 120 μA with 4 μA steps to compensate for bandwidth variations of the PLL. The closed-loop bandwidth of the PLL is designed to 60 kHz, and the phase margin is about 60°.

V. MEASUREMENT RESULTS

The receiver chip was fabricated in a 0.13 μm one-poly-eight-metal (1P8M) CMOS process. It occupies a total silicon area of less than 4 mm² including all ESD pads. The chip is housed in a 5 × 5 mm² 32-pin QFN package. A micrograph of the die is shown in Fig. 16. The measured performance referred to the SMA connector input is summarized in Table III. The measured NF ranges from 5 dB to 5.8 dB in the L-band. The measured phase noise spectrum at the receiver output is as shown in Fig. 17. The PLL locking range is measured under all process, temperature, and supply variation conditions and exceeds the required 1.8–4.5 GHz range. Measured frequency tuning curves are shown in Fig. 18. The measured cut-off frequency deviation error of the receiver before and after AFT is shown in Fig. 19. It indicates that the presented AFT method can guarantee widely
Tunable achievement and high precision for the LPF. The cut-off frequency deviation after AFT is less than 6% and even less than 3% within the high bandwidth frequency range.

The stated IIP2 is measured, applying two-tone frequencies at 100 MHz and 105 MHz away from the desired frequency, whereas, for IIP3, a two-tone test with blockers at 100 MHz

### TABLE III

<table>
<thead>
<tr>
<th>Performance</th>
<th>Measured</th>
<th>Requirements</th>
</tr>
</thead>
<tbody>
<tr>
<td>$S_{11}$ (dB)</td>
<td>&lt;-10.5</td>
<td>-</td>
</tr>
<tr>
<td>Gain Max/Min/Step (dB)</td>
<td>89.5/40.5</td>
<td>-</td>
</tr>
<tr>
<td>NF @ Max gain (dB)</td>
<td>Receiver 5-5.8</td>
<td>7.2</td>
</tr>
<tr>
<td></td>
<td>Baseband &lt;33.5</td>
<td>&lt; 35</td>
</tr>
<tr>
<td>IIP2 @ Max gain (dBm)</td>
<td>Receiver 27.5</td>
<td>&gt; 10</td>
</tr>
<tr>
<td></td>
<td>Baseband 45</td>
<td>&gt; 40</td>
</tr>
<tr>
<td>IIP3 @ Max gain (dBm)</td>
<td>Receiver -7.5</td>
<td>&gt; -12.5</td>
</tr>
<tr>
<td></td>
<td>Baseband 18</td>
<td>&gt; 14</td>
</tr>
<tr>
<td>Filter rejection with 10 MHz BW @ 20 MHz (dB)</td>
<td>25</td>
<td>&gt; 20</td>
</tr>
<tr>
<td>DC offset (mV)</td>
<td>&lt; 3.0</td>
<td>-</td>
</tr>
<tr>
<td>Power consumption (mW)</td>
<td>156.8 @ 2.8 V</td>
<td>-</td>
</tr>
<tr>
<td>Die size (mm$^2$)</td>
<td>4 @ 0.13 μm CMOS</td>
<td>-</td>
</tr>
<tr>
<td>I/Q amplitude balance (dB)</td>
<td>0.2</td>
<td>-</td>
</tr>
<tr>
<td>I/Q phase balance (Deg)</td>
<td>0.3</td>
<td>-</td>
</tr>
<tr>
<td>PLL tuning range (GHz)</td>
<td>1.7-4.8</td>
<td>1.8-4.5</td>
</tr>
<tr>
<td>Phase noise integrated (100 Hz – 4 MHz) (Deg)</td>
<td>1</td>
<td>-</td>
</tr>
<tr>
<td>Sensitivity (dBm)</td>
<td>-92.2 @ 4.42 Ms/s, QPSK 1/2</td>
<td>9 dB CNR</td>
</tr>
<tr>
<td></td>
<td>-89.1 @ 4.42 Ms/s, QPSK 3/4</td>
<td></td>
</tr>
<tr>
<td></td>
<td>-81.9 @ 45 Ms/s, 8PSK 3/4</td>
<td></td>
</tr>
<tr>
<td></td>
<td>-80.5 @ 45 Ms/s, 8PSK 7/8</td>
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### TABLE IV

<table>
<thead>
<tr>
<th>Ref.</th>
<th>[2]</th>
<th>[4]</th>
<th>[10]</th>
<th>[31]</th>
<th>This work</th>
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<tbody>
<tr>
<td>Technology</td>
<td>65 nm CMOS</td>
<td>0.13 μm CMOS</td>
<td>0.18 μm CMOS</td>
<td>45 nm CMOS</td>
<td>0.13 μm CMOS</td>
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<tr>
<td>Power (mW)</td>
<td>135</td>
<td>103</td>
<td>500</td>
<td>60-230</td>
<td>156.8</td>
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<tr>
<td>Voltage (V)</td>
<td>-</td>
<td>1.2</td>
<td>1.8/2.5</td>
<td>1.1</td>
<td>2.8</td>
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<tr>
<td>Die size (mm$^2$)</td>
<td>7</td>
<td>7.2</td>
<td>7.56</td>
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<tr>
<td>Freq. range (MHz)</td>
<td>170-1700</td>
<td>470-1675</td>
<td>950-2150</td>
<td>100-5000</td>
<td>900-2250</td>
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<tr>
<td>Gain Max/Min/Step (dB)</td>
<td>94.5/2.5/0.5</td>
<td>100/100/0.5</td>
<td>90/10/1</td>
<td>64-84/1</td>
<td>89.5/4.05</td>
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<tr>
<td>RF/MM range (MHz)</td>
<td>20/72</td>
<td>30/63.5</td>
<td>-</td>
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<td>18/67.5</td>
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<td>BW range a (MHz)</td>
<td>0.1-7 (D)</td>
<td>2-5 (D)</td>
<td>BW channel &gt; 40</td>
<td>0.5-20 (D)</td>
<td>4.5-32 (C)</td>
</tr>
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<td>BW precision</td>
<td>0.5%</td>
<td>3%</td>
<td>-</td>
<td>&lt; 5%</td>
<td>&lt; 6% (4.5-15 MHz)</td>
</tr>
<tr>
<td>WR &amp; HP b</td>
<td>No</td>
<td>No</td>
<td>-</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>DC offset (mV)</td>
<td>6</td>
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<td>-</td>
<td>-</td>
<td>3</td>
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<td>Calibration scheme c</td>
<td>Analog</td>
<td>Analog</td>
<td>-</td>
<td>Digital</td>
<td>Digital</td>
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<tr>
<td>NF @ Max gain (dB)</td>
<td>4.3</td>
<td>2.5-3.5</td>
<td>12</td>
<td>2.3-6.5</td>
<td>5-5.8</td>
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<tr>
<td>NF @ RF backoff d (dB)</td>
<td>-</td>
<td>13</td>
<td>-</td>
<td>-</td>
<td>10.3</td>
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<tr>
<td>IIP2 @ Max gain (dBm)</td>
<td>25</td>
<td>27</td>
<td>-</td>
<td>-</td>
<td>27.5</td>
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<td>IIP2 @ RF backoff (dBm)</td>
<td>35</td>
<td>46</td>
<td>-</td>
<td>30-36 @ Min gain</td>
<td>40</td>
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<tr>
<td>IIP3 @ Max gain (dBm)</td>
<td>-13</td>
<td>-12</td>
<td>-</td>
<td>-</td>
<td>-7.5</td>
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<tr>
<td>IIP3 @ RF backoff (dBm)</td>
<td>-7</td>
<td>8</td>
<td>12.6 @ Min gain</td>
<td>-18 (-3) @ Min gain</td>
<td>2.5</td>
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<tr>
<td>PN integrated</td>
<td>1.1</td>
<td>1</td>
<td>0.6</td>
<td>&lt; 1</td>
<td>1</td>
</tr>
</tbody>
</table>

a D: discrete; C: continuous;  
b Wide band range and high BW precision;  
c For DCOC;  
d Max RF backoff are equal to 15 dB, 10 dB, 31 dB and 18 dB respectively.
and 195 MHz offset is performed. The plot in Fig. 20 shows the measured and required linearity performance of the receiver when the receiver works in the AGC mode. The measured IIP2 and IIP3 both exceed the desired target with the minimum difference in excess of 7 dBm when the input power is varied between –85 and –5 dBm.

The CNR plot at the receiver output, obtained by calculation of the constellation error of the digital demodulator for different input powers and with the AGC loop running in real time, is depicted in Fig. 21. There, an input signal using a QPSK 1/2 modulation scheme is applied with a symbol rate of 4.42 Ms/s. The CNR achieved is better than 20 dB from –80 to –5 dBm, and the peak CNR exceeds 37 dBm, allowing for robust operation in a mobile environment. In continuous receive mode, the receiver consumes about 56 mA at 2.8 V supply.

Compared with previously reported work related to DBS receivers, as shown in Table IV, this work achieves minimum chip area, continuous and wide bandwidth range while maintaining comparable performance.

VI. CONCLUSION

A complete DVB-S/S2 and ABS-S RF TV receiver, utilizing a direct-conversion structure, has been implemented in a 0.13 μm CMOS technology providing widely-tunable performance and digitally-assisted calibration. On the basis of combined system and circuit design techniques, this receiver complies with stringent noise and linearity specifications with state-of-the-art implementations and silicon area of less than 4 mm². Moreover, the receiver does not require off-chip balun and matching networks, and integrates all functional modules. Low BOM as well as small PCB size are achieved, requiring a minimum number of external components.

REFERENCES


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